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KEITHLEY

Model 7072 Semiconductor Matrix Card Instruction Manual

Contains Operating and Servicing Information

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SAFETY PRECAUTIONS

The following safety precautions should be observed before using the Model 7072 and the associated instruments.

This matrix card is intended for use by qualified personnel who recognize shock hazards and are familiar with the safety precautions required to avoid possible injury. Read over this manual carefully before using the matrix card.

Exercise extreme caution when a shock hazard is present at the test circuit. User-supplied lethal voltages may be present on the card connector jacks. The American National Standards Institute (ANSI) states that a shock hazard exists when voltage levels greater than 30V RMS or 42.4V peak are present. A good safety practice is to expect that hazardous voltage is present in any unknown circuit before measuring.

Do not exceed 200V between any two pins or between any pin and earth ground.

Inspect the connecting cables and test leads for possible wear, cracks, or breaks before each use.

For maximum safety, do not touch the test cables or any instruments while power is applied to the circuit under test. Turn off the power and discharge any capacitors before connecting or disconnecting cables from the matrix card.

Do not touch any object which could provide a current path to the common side of the circuit under test or power line (earth) ground. Always make measurements with dry hands while standing on a dry, insulated surface capable of withstanding the voltage being measured.

Do not exceed the maximum allowable input of the matrix card, as defined in the specifications and operation section of this manual.

SPECIFICATIONS

Rows:	Low Current (A - B)	General Purpose (C - F)	C-V (G - H)
CROSSPOINT CONFIGURATION:	2-pole Form A	2-pole Form A	1-pole Form A, Common Guard
OFFSET CURRENT:	<1 pA	<20 pA	<20 pA
PATH ISOLATION:			
Resistance:	$>10^{13}\ \Omega$	$>10^{12}\ \Omega$	$>10^{12}\ \Omega$
Capacitance (nominal):	0.4 pF	1 pF	0.6 pF
1 MHz, 1 MΩ load (typical):	50dB	40 dB	50 dB
3dB BANDWIDTH (typical), 1MΩ Load:	15 MHz	8 MHz	5 MHz
RELAY DRIVE CURRENT (per crosspoint):	40 mA	60 mA	80 mA

MATRIX CONFIGURATION: 8 rows by 12 columns.

CONNECTOR TYPE: Three lug triaxial (Signal, Guard, Chassis).

MAXIMUM SIGNAL LEVEL: 200V, 1A carry/ 0.5A switched, 10VA peak (resistive load).

COMMON MODE VOLTAGE: 200V maximum between any 2 pins or chassis.

CONTACT LIFE:

Cold Switching: 10^7 closures.

At Maximum Signal Level: 10^5 closures.

PATH RESISTANCE (per conductor): <1Ω initial, <3.5Ω at end of contact life.

CONTACT POTENTIAL: <20μV per crosspoint (Signal to Guard).

RELAY SETTLING TIME: <15ms.

INSERTION LOSS (1MHz, 50Ω source, 1MΩ load): 0.1dB typical.

ENVIRONMENT:

OFFSET CURRENT and PATH ISOLATION Specifications: 23°C, <60% R.H.

Operating: 0° to 50°C, up to 35°C at 70% R.H.

Storage: −25 to +65°C.

ACCESSORY SUPPLIED: Instruction manual.

ACCESSORIES AVAILABLE:

Model 7078-TRX-BNC: 3-Lug Triax to BNC Adapter

Model 7078-TRX-T: 3-Lug Triax Tee Adapter

Model 7078-TRX-3: 3-Lug Triax Cable, 0.9m (3 ft.)

Model 7078-TRX-10: 3-Lug Triax Cable, 3m (10 ft.)

Model 7078-TBC: 3-Lug Female Triax Bulkhead Connector with Cap

Model 7078-CSHP: Cable Set to connect 7072 to HP 4145

Specifications subject to change without notice.

Contains information on Model 7072 features, specifications, and accessories.

SECTION 1
General Information

Details installation of the Model 7072 Semiconductor Matrix Card within the Model 707 Switching Matrix, covers card connections, and also discusses measurement considerations.

SECTION 2
Operation

Gives four typical applications for the Model 7072, including combined quasistatic and high-frequency CV measurements, semiconductor switching matrix, van der Pauw resistivity measurements, and semiconductor parameter analysis.

SECTION 3
Applications

Contains performance verification procedures, troubleshooting information and principles of operation for the matrix card.

SECTION 4
Service Information

Lists replacement parts, and also includes component layout and schematic drawings for the Model 7072.

SECTION 5
Replaceable Parts

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SECTION 1
General Information

1.1 INTRODUCTION

This section contains general information about the Model 7072 Semiconductor Matrix Card. The Model 7072 is designed for flexibility in switching semiconductor test setups. Two low-current pathways, and two C-V pathways in addition to four general-purpose pathways allow complete system versatility.

Section 1 is arranged in the following manner:

1.2 Features
1.3 Warranty Information
1.4 Manual Addenda
1.5 Safety Symbols and Terms
1.6 Specifications
1.7 Unpacking and Inspection
1.8 Repacking for Shipment
1.9 Optional Accessories
1.10 Coaxial Jumper Access

1.2 FEATURES

Key features of the Model 7072 Semiconductor Matrix Card include:

- 8 × 12 (eight row by 12 column) switching matrix.
- Two rows (A and B) with low-current offset for low-current measurements.
- Two dedicated rows (G and H) for CV measurements.
- Three-lug triax connectors for all row and columns allow guarding of each signal pathway to minimize the effects of stray capacitance, leakage current, and leakage resistance.
- Model 7072 cards can be connected together to expand the number of columns in the matrix.

1.3 WARRANTY INFORMATION

Warranty information is located on the inside front cover of this instruction manual. Should your Model 7072 require warranty service, contact the Keithley representative or authorized repair facility in your area for further information. When returning the matrix card for repair, be sure to fill out and include the service form at the back of this manual in order to provide the repair facility with the necessary information.

1.4 MANUAL ADDENDA

Any improvements or changes concerning the matrix card or manual will be explained in an addendum included with the the unit. Be sure to note these changes and incorporate them into the manual before using or servicing the unit.

1.5 SAFETY SYMBOLS AND TERMS

The following symbols and terms may be found on an instrument or used in this manual.

The symbol on an instrument indicates that the user should refer to the operating instructions located in the instruction manual.

The symbol on an instrument shows that high voltage may be present on the terminal(s). Use standard safety precautions to avoid personal contact with these voltages.

The **WARNING** heading used in this manual explains dangers that might result in personal injury or death. Always read the associated information very carefully before performing the indicated procedure.

The **CAUTION** heading used in this manual explains hazards that could damage the matrix card. Such damage may invalidate the warranty.

1.6 SPECIFICATIONS

Model 7072 specifications may be found at the front of this manual. These specifications are exclusive of the matrix mainframe specifications, which are located in the Model 707 Instruction Manual.

1.7 UNPACKING AND INSPECTION

1.7.1 Inspection for Damage

Upon receiving the Model 7072, carefully unpack it from its shipping carton and inspect the card for any obvious signs of physical damage. Report any such damage to the shipping agent immediately. Save the original packing carton for possible future reshipment.

1.7.2 Shipment Contents

The following items are included with every Model 7072 order:

- Model 7072 Semiconductor Matrix Card.
- Model 7072 Instruction Manual.
- Coaxial jumper cables (4) for matrix expansion.
- Additional Accessories as ordered.

1.7.3 Instruction Manual

The Model 7072 Instruction Manual is three-hole drilled so that it can be added to the three-ring binder of the Model 707 Switching Matrix Instruction Manual. After removing the plastic wrapping, place the manual in the binder after the mainframe instruction manual. Note that a manual identification tab is included and should precede the matrix card instruction manual.

If an additional instruction manual is required, order the manual package, Keithley part number 7072-901-00. The manual package includes an instruction manual and any pertinent addenda.

1.8 REPACKING FOR SHIPMENT

Should it become necesary to return the Model 7072 for repair, carefully pack the card in its original packing carton or the equivalent, and include the following information:

- Advise as to the warranty status of the matrix card.
- Write ATTENTION REPAIR DEPARTMENT on the shipping label.
- Fill out and include the service form located at the back of this manual.

1.9 OPTIONAL ACCESSORIES

The following accessories are available to make connections to the Model 7072.

Model 6171 3-slot Male to 2-lug Female Triaxial Adapters—The Model 6171 allows male 2-lug triaxial cables to be connected to the Model 7072.

Model 7078-TRX-T 3-Lug Triax Tee Adapter—The Model 7078-TRX-T allows multiple triax connections to the Model 7072 column or row jacks.

Model 7078-TRX-BNC 3-Lug Triax to BNC Adapter—The Model 7078-TRX-BNC allows BNC cables to be connected to the Model 7072.

Model 7078-TRX Triaxial Cables—The Model 7078-TRX cables are terminated with 3-slot male triaxial connectors. The Model 7078-TRX-3 is 0.9m (3 ft.) in length, and the Model 7078-TRX-10 is 3m (10 ft.) long.

Model 7078-TBC 3-Lug Female Triax Bulkhead Connector with Cap—The Model 7078-TBC can be used for applications such as test fixtures.

Model 7078-CSHP Cable Set—The Model 7078-CSHP Cable Set includes the necessary cables and adapters to connect the Model 7072 to the Hewlett-Packard Model 4145 Semiconductor Parameter Analyzer. The Model 7078-CSHP includes four Model 7078-TRX-10 10ft. 3-lug triaxial cables, four Model 7051-10 10ft. BNC cables, and four Model 7078-TRX-BNC 3-lug triax to BNC adapters.

1.10 COAXIAL JUMPER ACCESS

Coaxial jumpers can be installed to expand rows A, B, G and H of the matrix using two or more Model 7072 Cards. An access door on the mainframe allows access to these jumpers. To allow access when the Model 707 is mounted in a rack, it is recommended that the Model 7079 Slide Rack Mount Kit be used.

SECTION 2
Operation

2.1 INTRODUCTION

This section contains information on matrix card connections, installation and matrix programming, and is arranged as follows:

2.2 **Handling Precautions:** Discusses precautions that should be taken when handling the card to avoid contamination that could degrade performance.

2.3 **Environmental Considerations:** Outlines environmental aspects of using the Model 7072.

2.4 **Card Installation and Removal:** Details installation in and removal from the Model 707 Switching Matrix mainframe.

2.5 **Connections:** Discusses card connectors, cables and adapters, and typical connections to other instrumentation.

2.6 **Matrix Configuration:** Discusses the switching matrix, as well as matrix expansion by connecting two or more cards together.

2.7 **Measurement Considerations:** Reviews a number of considerations when making low-level current and capacitance measurements.

2.2 HANDLING PRECAUTIONS

To maintain high impedance isolation, care should be taken when handling the matrix card to avoid contamination from such foreign materials as body oils. Such contamination can substantially lower leakage resistances, degrading performance. The areas of the card that are most sensitive to contamination are those associated with the Teflon® insulators. To avoid any possible contamination, always grasp the card by the handle or the card edges. Do not touch board surfaces, components, or card edge connectors.

Dirt build-up over a period of time is another possible source of contamination. To avoid this problem, operate the mainframe and matrix card only in a clean environment. If contamination is suspected,clean the card as discussed in Section 4. Also, the performance verification procedures in Section 4 can be used to test the card for low leakage resistances that could signal contamination.

2.3 ENVIRONMENTAL CONSIDERATIONS

For rated performance, the card should be operated within the temperature and humidity limits given in the specifications at the front of this manual. Note that current offset and path isolation values are specified within a lower range of limits than the general operating environment.

2.4 CARD INSTALLATION AND REMOVAL

Before making connections, the Model 7072 should be installed within the Model 707 Switching Matrix, as summarized below. Figure 2-1 shows the installation procedure.

WARNING

Turn off the mainframe power and disconnect the line cord before installing or removing matrix cards.

NOTE

The SMB coaxial jumpers used to expand the matrix with two or more Model 7072 cards need not be installed before card insertion; an access door on top of the mainframe allows access to the SMB connectors after the card is installed.

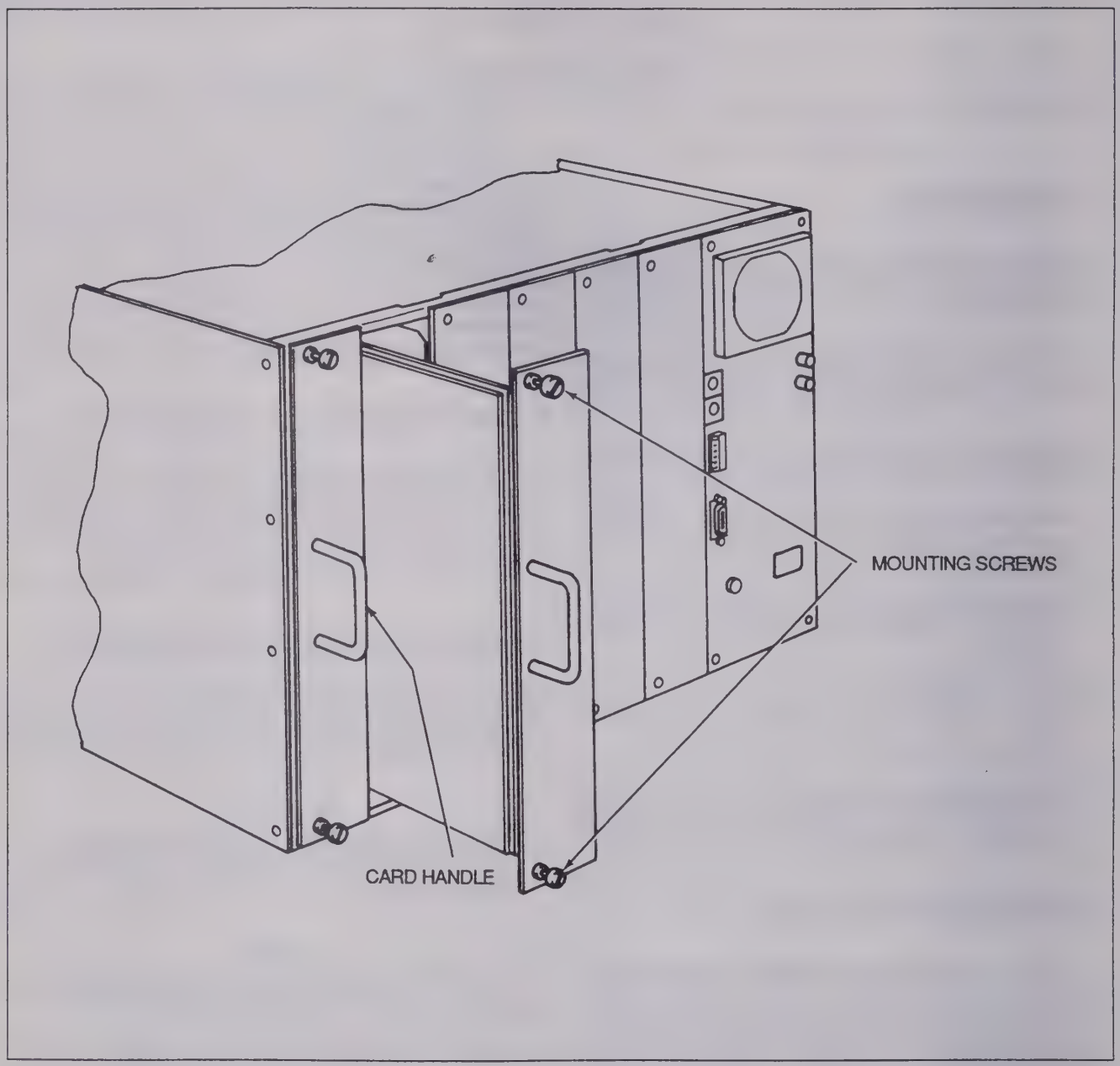


Figure 2-1. Model 7072 Installation

1. Before installing the card, make sure the access door on top of the Model 707 is fully closed and secured. The access door contains tracks for the card slots and must be in place to properly install the card.
2. With one hand grasping the handle, and the other holding the bottom of the card, line up the card with the tracks in the desired slot. Make certain that the component side of the card is facing the fan on the mainframe.

CAUTION

Do not touch the card surfaces or any components to avoid contamination that could degrade card performance.

3. Slide the card into the mainframe until it is properly seated in the edge connectors at the back of the slot. Once the card is properly seated, secure it to the mainframe by finger tightening the spring-loaded screws.

WARNING

The mounting screws must be secured to ensure a proper chassis ground connection between the card and the mainframe. Failure to properly secure this ground connection may result in personal injury or death due to electric shock.

4. To remove a card, first turn off the power and disconnect the line cord from the mainframe. Disconnect all external and internal cables (internal cables can be reached through the access door). Loosen the mounting screws, then pull the card out of the mainframe by the handle. When the back edge of the card clears the mainframe, support it by grasping the bottom edge near the back edge.

2.5 CONNECTIONS

Card connectors, recommended cables and adapters, and typical connections to test instruments are discussed in the following paragraphs.

2.5.1 Card Connectors

The card connectors are shown in Figure 2-2. Each row and column is equipped with a 3-lug female triax connector. As shown in Figure 2-3, the center conductor is SIGNAL, the inner shield is GUARD, and the outer shield, or shell is chassis ground. Note that 3-lug connectors are used to avoid possible damage from inadvertently attempting to connect BNC cables.

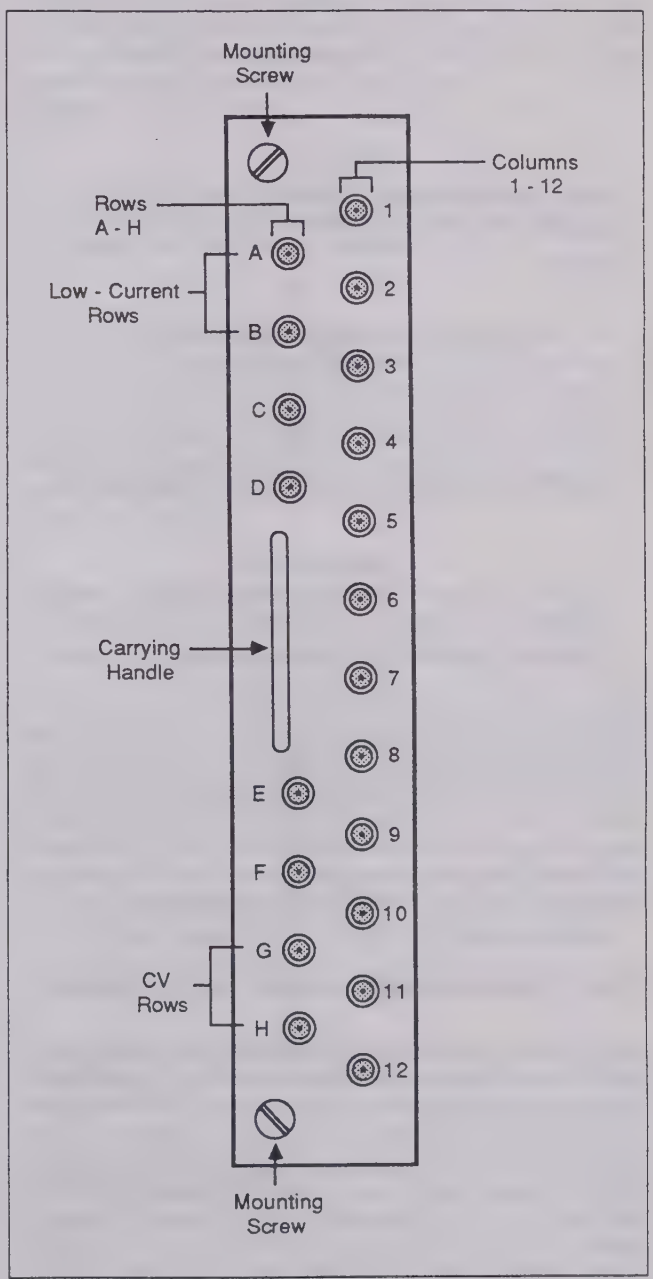


Figure 2-2. Card Connectors

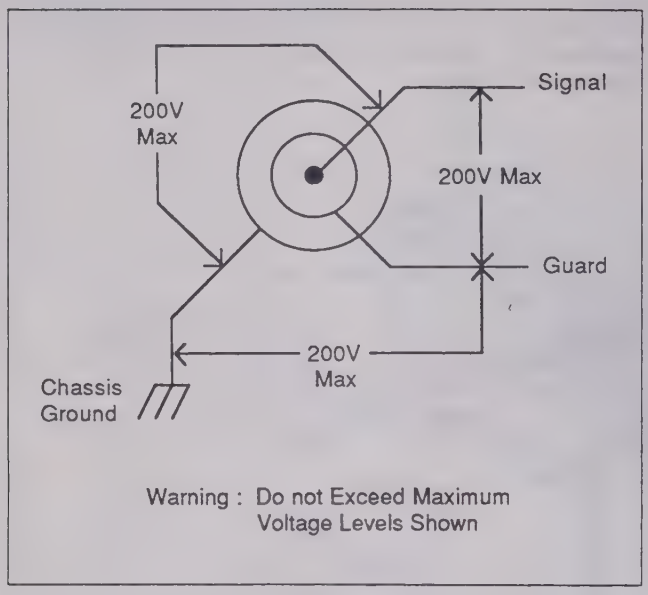


Figure 2-3. Triax Connector Configuration

WARNING
Do not exceed 200V between SIGNAL and GUARD, or between SIGNAL and chassis ground, or GUARD and chassis ground.

The Model 7072 has 12 columns that are labelled 1 through 12, as well as eight rows, A through H. Rows A and B are labelled LOW I and are intended for low-current measurements. Rows G and H are labelled CV and are designed for capacitance-voltage measurements. Rows C through F are general purpose rows that can be used for ordinary voltage, current, or resistance measurements.

2.5.2 Recommended Cables and Adapters

Table 2-1 summarizes the cables and adapters recommended for use with the Model 7072. Equivalent user-supplied items may be substituted as long as they are of sufficient quality (low offset current, high leakage resistance). Using substandard cables and adapters may degrade the integrity of the measurements made using the matrix card. See paragraph 2.7 for a discussion of measurement considerations.

Table 2-1. Recommended Cables and Adapters

Description	Applications
6171 3-slot male to 2-lug female triax.	Connect 2-slot triax cable to 7072
6011 2-slot triax to alligator cable*	7072 input/output connections
7078-TRX-3, 7078-TRX-10 triax cables	7072 input/output connections
7078-TRX-T triax tee adapter	Daisy chain 7072 columns or rows
7078-TRX-BNC triax to BNC adapter	Connect BNC cables to 7072
7025 unterminated triax (2 slot)*	For custom 7072 connections
Guarded adapter (6167**)	Guarded current source

*Model 6171 adapter required to connect these cables to Model 7072

**6167 requires modification by disconnecting input LO internally.

2.5.3 Triaxial to Banana Plug Adapter Preparation

For instruments that use banana jacks, a special 3-slot triax-to-single banana plug must be prepared, as discussed below. This special cable can be prepared as outlined below using the parts listed in Table 2-2. Note that you can use either an unterminated triax cable, or cut a dual-connector cable (7078-TRX-10) in half to construct two cables. The steps for the procedure below are shown in Figure 2-4.

1. Using a knife, cut and strip back the outer insulation about 1½ inches.
2. Remove the outer insulation, then cut away the outer shield back as far as the insulation is stripped.
3. Carefully strip away the insulation over the inner shield one inch, then cut the inner shield off even with the stripped insulation.
4. Strip the inner conductor ½ inch, then twist the strands together.
5. Unscrew the cover from a banana plug, then slide the cover over the center conductor of the triax cable.
6. Insert the stripped center conductor through the hole in the body of the banana plug, then wrap the wire around the plug body.
7. Screw on the plastic cover, and make certain the wire is secure by gently pulling on the plug.

Table 2-2. Parts for Special Triaxial Cable

Keithley Part or Model Number	Description
7078-TRX-3 triax cable*	Unterminated 3-slot triax cable
Part # B6-10-2	Red banana plug

*One connector must be cut off

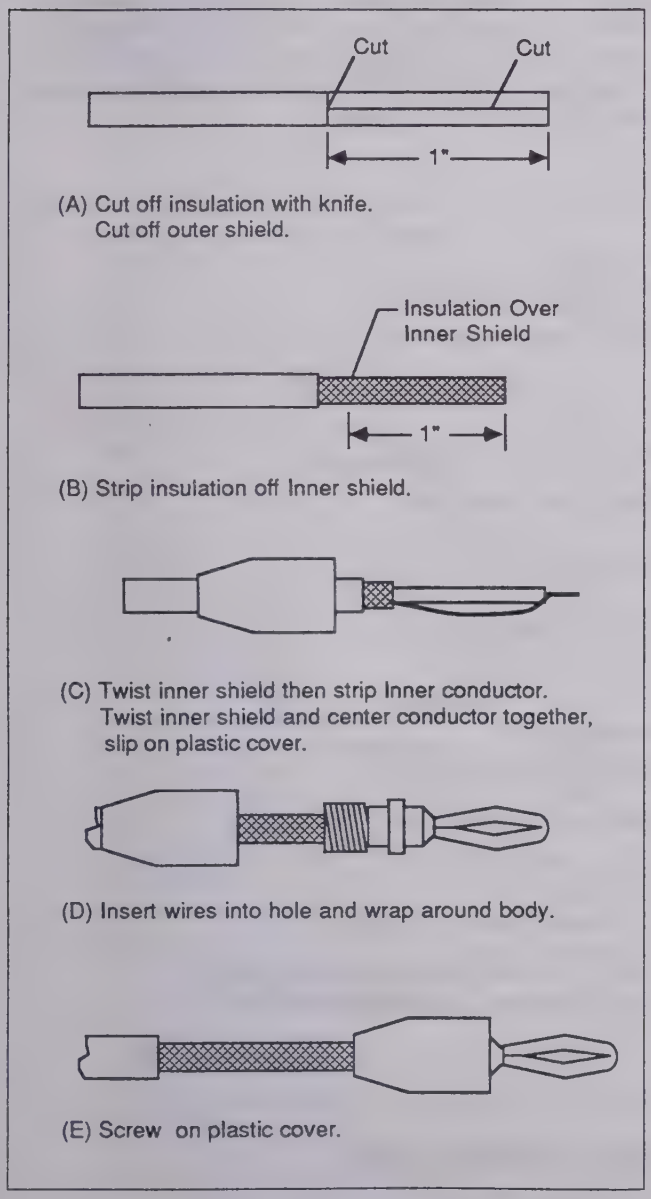

Cut
Cut
1"
(A) Cut off insulation with knife.
Cut off outer shield.
Insulation Over
Inner Shield
1"
(B) Strip insulation off Inner shield.
(C) Twist inner shield then strip Inner conductor.
Twist inner shield and center conductor together,
slip on plastic cover.
(D) Insert wires into hole and wrap around body.
(E) Screw on plastic cover.

Figure 2-4. Triaxial Cable Preparation

2.5.4 General Instrument Connections

The following paragraphs discuss connecting the Model 7072 to various general classes of instrumentation such as DMMs, electrometers, sources, and source/measure units. Because these configurations are generic in nature, some modification of the connecting schemes may be necessary for your particular instrumentation. Also, special cables or adapters may be necessary. In all cases, 3-lug triax cables must be used to make the connections.

WARNING

Do not use coaxial cables and adapters because hazardous voltage from guard sources may be present on the cable shields.

Figure 2-5 shows the general instrument connections for the discussions below. Note that DUT guarding or shielding are not indicated here; see Figures 2-21 and 2-24 for shielding and guarding information. Also, 2-pole switching for rows A-F is shown in the figures; GUARD is not switched on rows G and H. As shown, all figures assume instruments are connected to rows, and the DUT is connected to columns.

DMM Connections

General DMM connections are shown in Figure 2-5(A), (B), and (C). Floating connections are shown in (A), with LO and HI routed to two separate jacks on the Model 7072. The common LO connections in (B) should be used only for non-critical applications because the performance of the GUARD pathway is not specified.

WARNING

Hazardous voltage from other guard sources may be present on LO or the DUT if other crosspoints are closed.

4-wire DMM connections are shown in Figure 2-5(C). In this case, a total of four jacks are required; HI, LO, SENSE HI, and SENSE LO.

Electrometer Connections

Typical electrometer connections are shown in Figure 2-5(D) through (G). The unguarded volts connections in (D) show the HI signal path routed through one jack, and the LO path goes through the other connector. Both GUARD pathways are connected to electrometer LO. For guarded voltage (E), Model 7072 GUARD is connected to electrometer GUARD.

The connections for electrometer fast amps and resistance measurements are shown in Figures 2-5(F) and (G). These configurations are essentially the same as those discussed above. For the case of fast amps, both GUARD paths are connected to electrometer LO, while in the case of guarded resistance, one GUARD path is connected to electrometer GUARD, and the other GUARD path is connected to electrometer LO.

Source Connections

Voltage and current source connections are shown in Figures 2-5(H) through (J). The HI and LO paths of the voltage source (H) are routed through two jacks, with both card GUARD pathways connected to voltage source LO. For the unguarded current source connections (I), card GUARD is again connected to source LO, with source HI and LO routed through two pathways. In the case of the guarded current source in (J), card GUARD of the HI signal path is connected to source GUARD, and the other GUARD path is connected to source LO.

Source/Measure Unit Connections

Figure 2-5(J) shows typical connections for a source/measure unit (SMU). In this instance, a remote-sensing type of a SMU is shown, requiring a total of four signal pathways to the DUT. For critial measurements, both source and sense HI pathways would be guarded as shown, with two of the four card GUARD pathways connected to SMU GUARD terminals. As with other instrument connections, the LO card GUARD pathways are connected to SMU LO terminals.

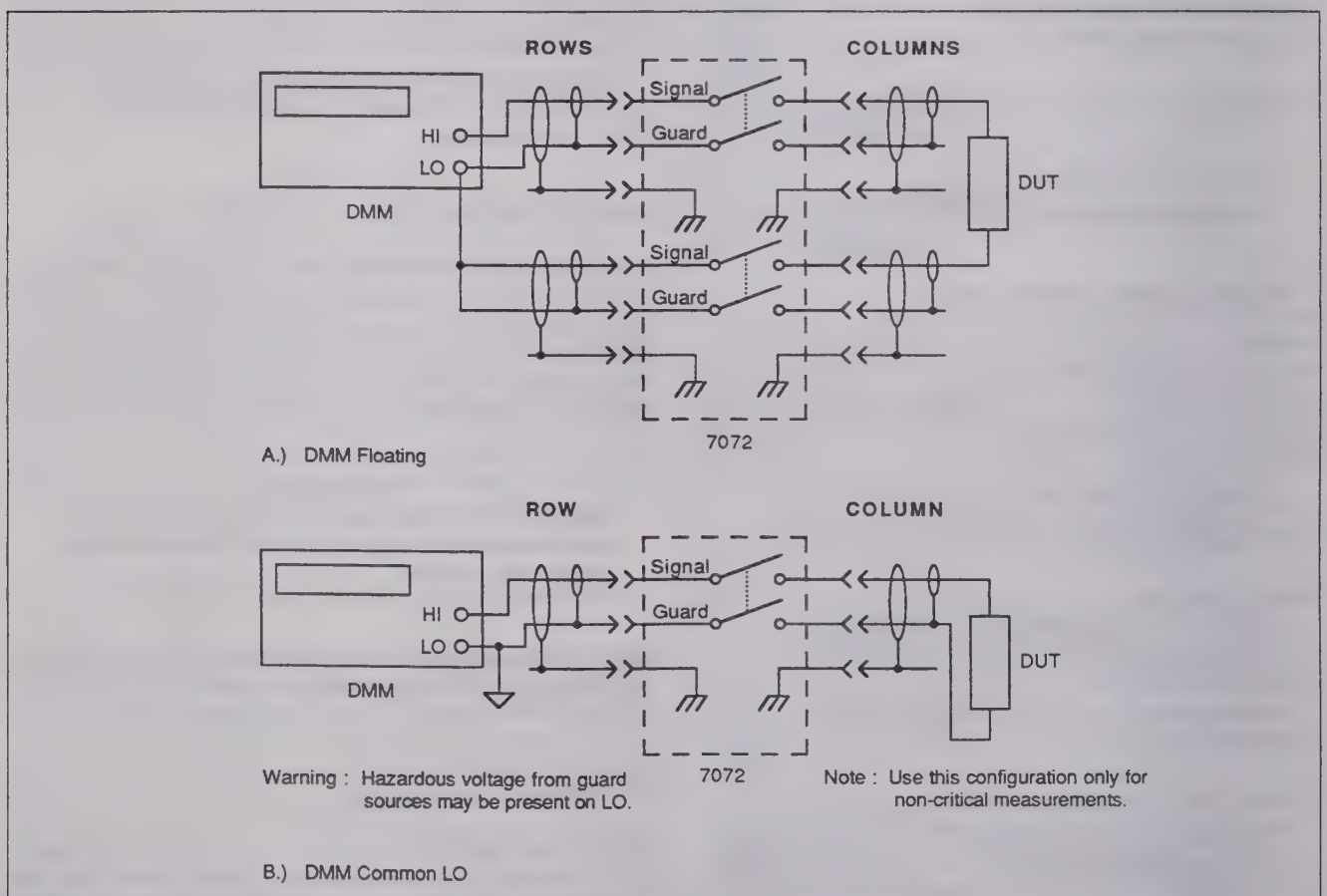


Figure 2-5. General Instrument Connections (A-B)

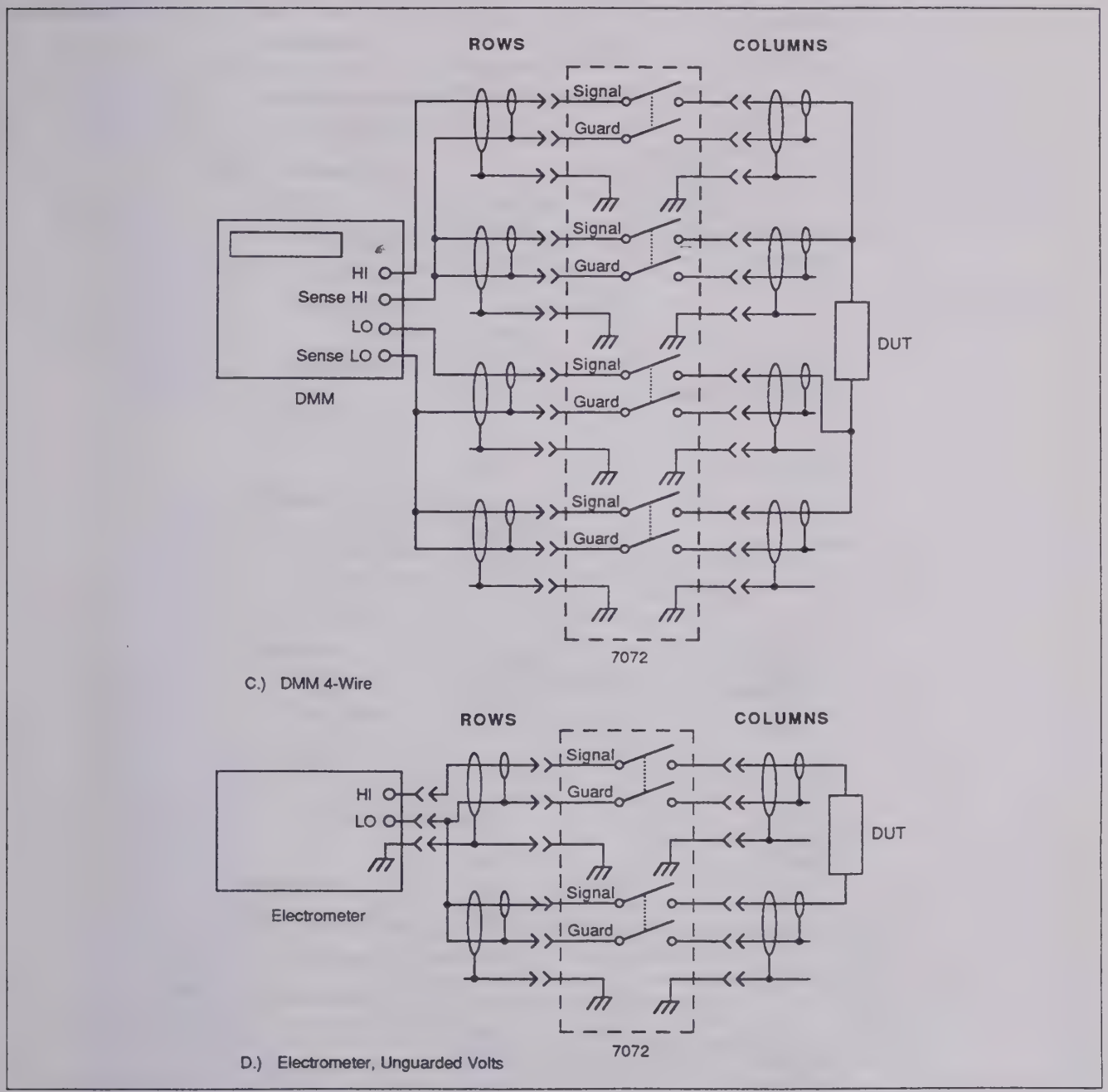
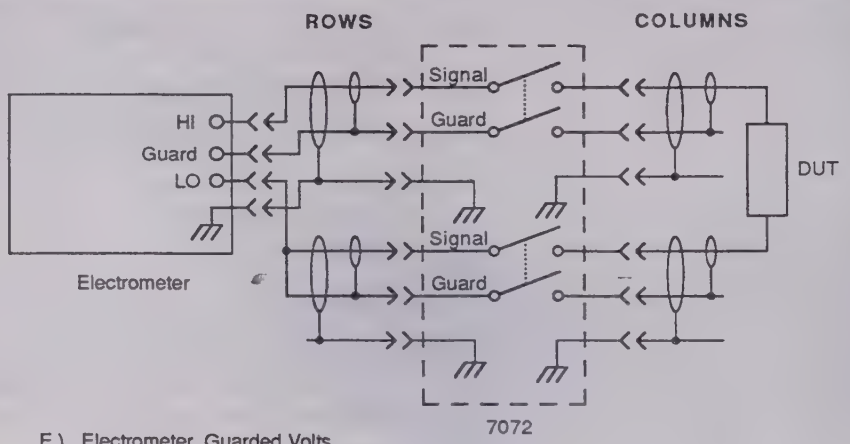
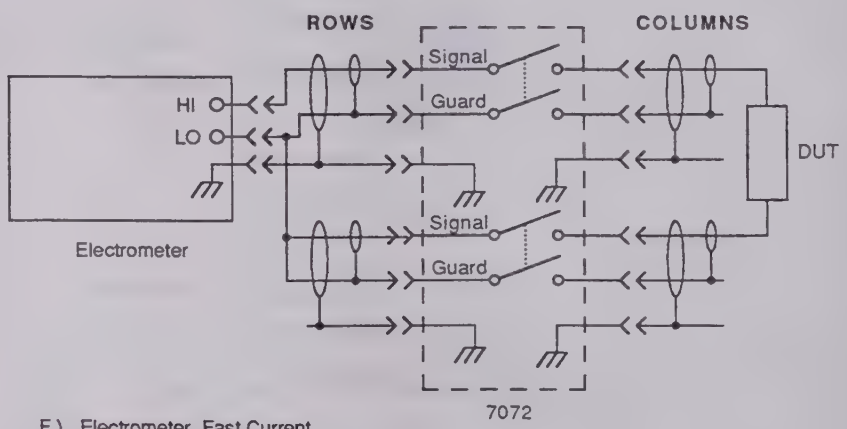


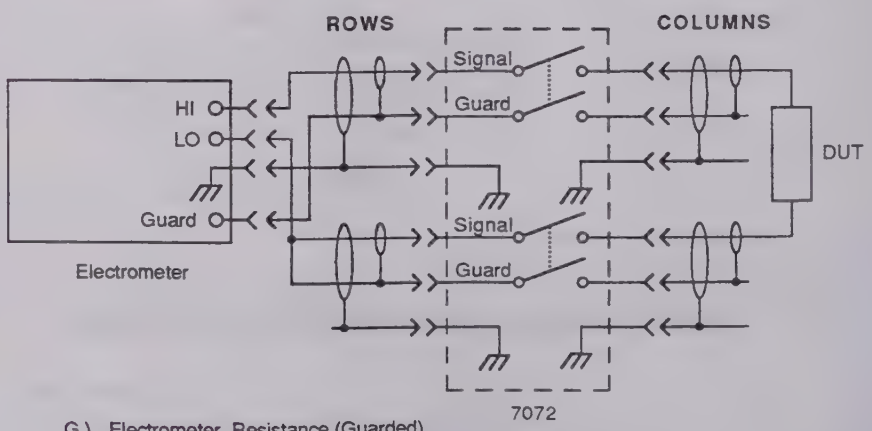
Figure 2-5. General Instrument Connections (C-D)



E.) Electrometer, Guarded Volts

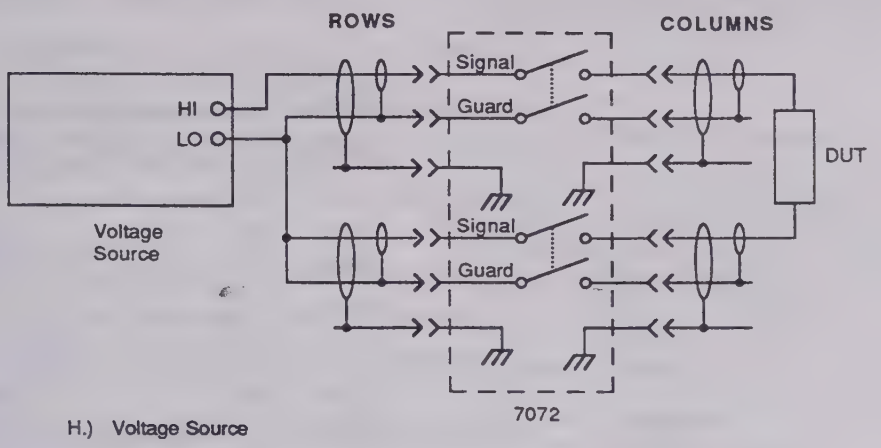


F.) Electrometer, Fast Current

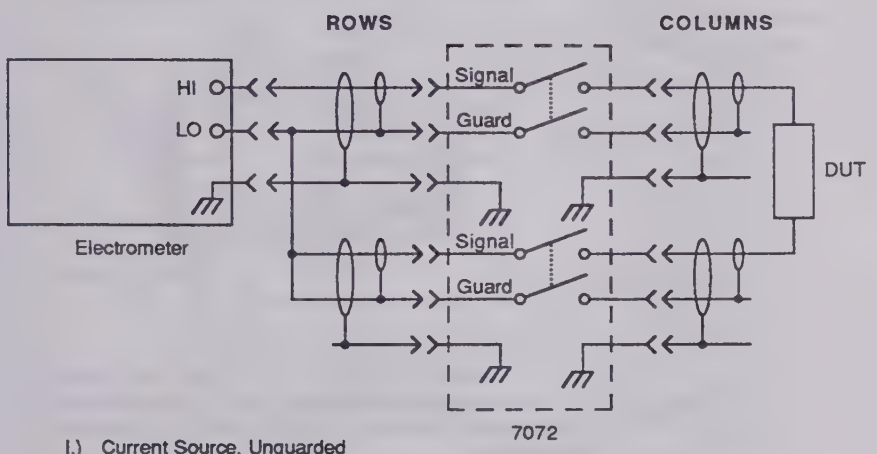


G.) Electrometer, Resistance (Guarded)

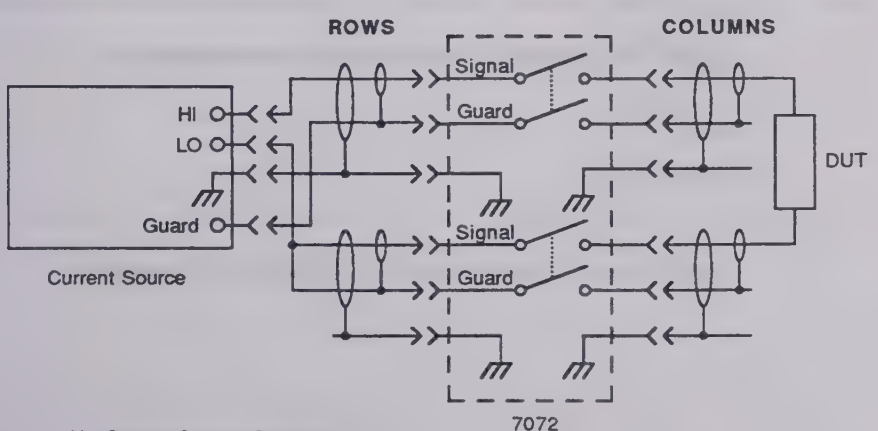
Figure 2-5. General Instrument Connections (E-G)



H.) Voltage Source

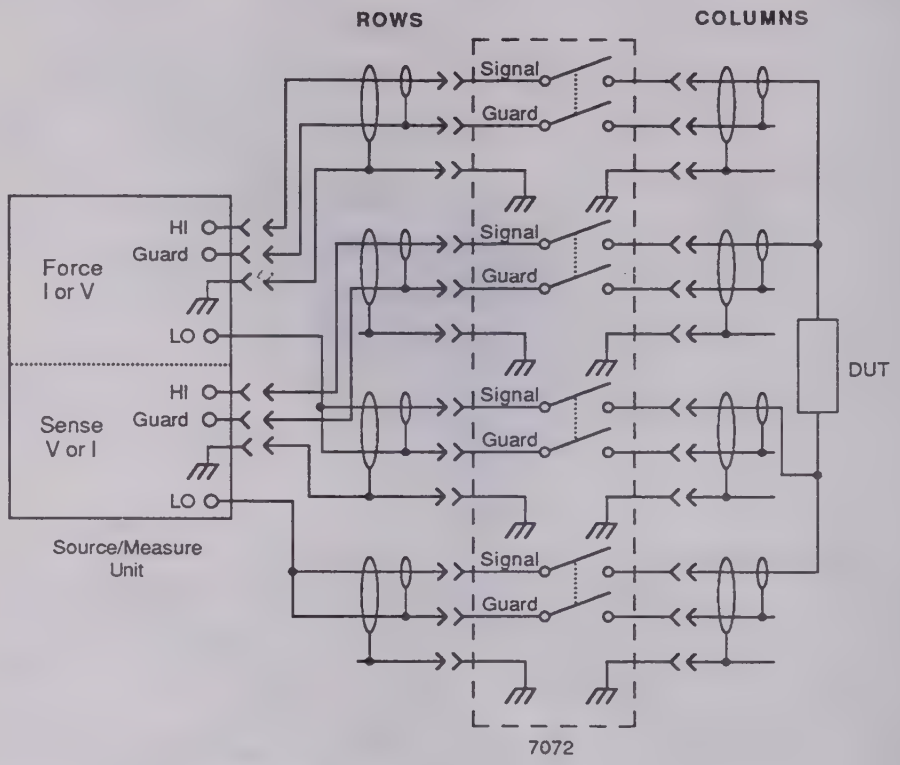


I.) Current Source, Unguarded



J.) Current Source, Guarded

Figure 2-5. General Instrument Connections (H-J)



K.) Source/Measure Unit

Notes : 1.) DUT shielding/guarding not shown. See figures 2-21 and2-24.
2.) 2-Pole switching for rows A-F shown. GUARD is not switched on rows G and H.

Figure 2-5. General Instrument Connections (K)

2.5.5 Keithley Instrument Connections

The following paragraphs outline connecting typical Keithley instruments to the Model 7072 Semiconductor Matrix Card. Other similar instruments can be connected using the same cabling as long as their input/output configurations are the same. Instrument connections covered include:

- Model 617 Electrometer/Source
- Model 196 DMM
- Model 230 Programmable Voltage Source
- Model 220 Programmable Current Source
- Model 590 CV Analyzer

Model 617 Electrometer Connections

Connections for the Model 617 Electrometer are shown in Figure 2-6. The electrometer INPUT should be connected only to rows A and B for currents less than 2nA; otherwise, current offset will affect measurement accuracy.

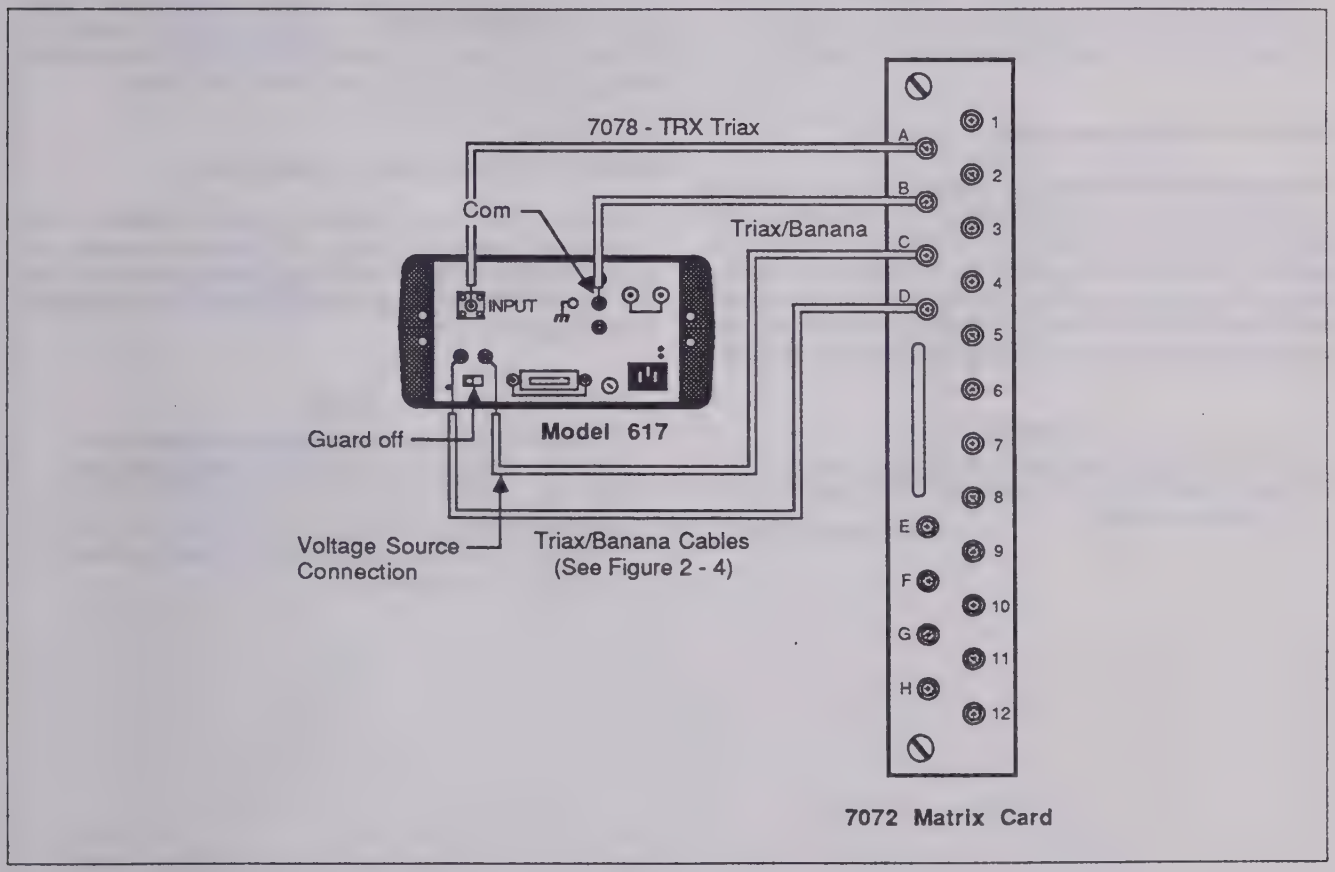


Figure 2-6. Model 617 Electrometer Connections

1. Connect one end of a Model 7078-TRX-3 or -10 3-lug triaxial cable to row A of the Model 7072.
2. Connect the other end of the triax cable to the Model 617 INPUT connector.
3. Connect the triax end of a prepared triax/banana cable to row B of the Model 7072.
4. Connect the banana plug end of the triax/banana cable to the COM terminal of the Model 617. The shorting link between COM and chassis ground should be removed for this application.
5. Place the GUARD switch in the OFF position.
6. To connect the voltage source to the Model 7072, connect the V-SOURCE HI and LO connectors of the Model 617 to the desired row connectors on the matrix card. Figure 2-6 shows connections to rows C and D.

Model 196 DMM Connections

Connect the Model 196 or other similar DMM to the matrix card using the general configuration shown in Figure 2-7. The VOLTS OHMS HI and LO terminals should be connected to the desired rows using the prepared triax/banana cables discussed above. For 4-wire ohms measurements, the OHMS SENSE HI and LO terminals should be connected to two addtional rows using the same type of cables.

NOTE

For low-level voltage measurements, connect the inner shield of the HI cable to VOLT OHMS LO to minimize noise.

Model 230 Voltage Source Connections

Connect the Model 230 OUTPUT and COMMON terminals to the desired rows using the prepared triax/banana plug cables, as shown in Figure 2-8. For remote sensing applications, the SENSE OUTPUT and SENSE COMMON connectors can be routed through two additional rows using similar cables.

Model 590 CV Analyzer Connections

The Model 590 CV Analyzer should be connected to rows G and H (CV rows), or any column as shown in Figure 2-9. The BNC cables that are supplied with the Model 590 can be used; however, Model 7078-TRX-BNC triax-to-BNC adapters must be used at the Model 7072 end.

Model 220 Current Source Connections

The Model 220 Current Source can be connected to the matrix card using the Model 6167 Guarded Adapter, as shown in Figure 2-10. This configuration guards the output signal to minimize the effects of distributed capacitance and leakage current.

NOTE

The Model 6167 Adapter must be modified by internally disconnecting the inner shield connection of the input jack from the GUARDED/ UNGUARDED selection switch. Otherwise, instrument LO will be connected to chassis ground through the adapter.

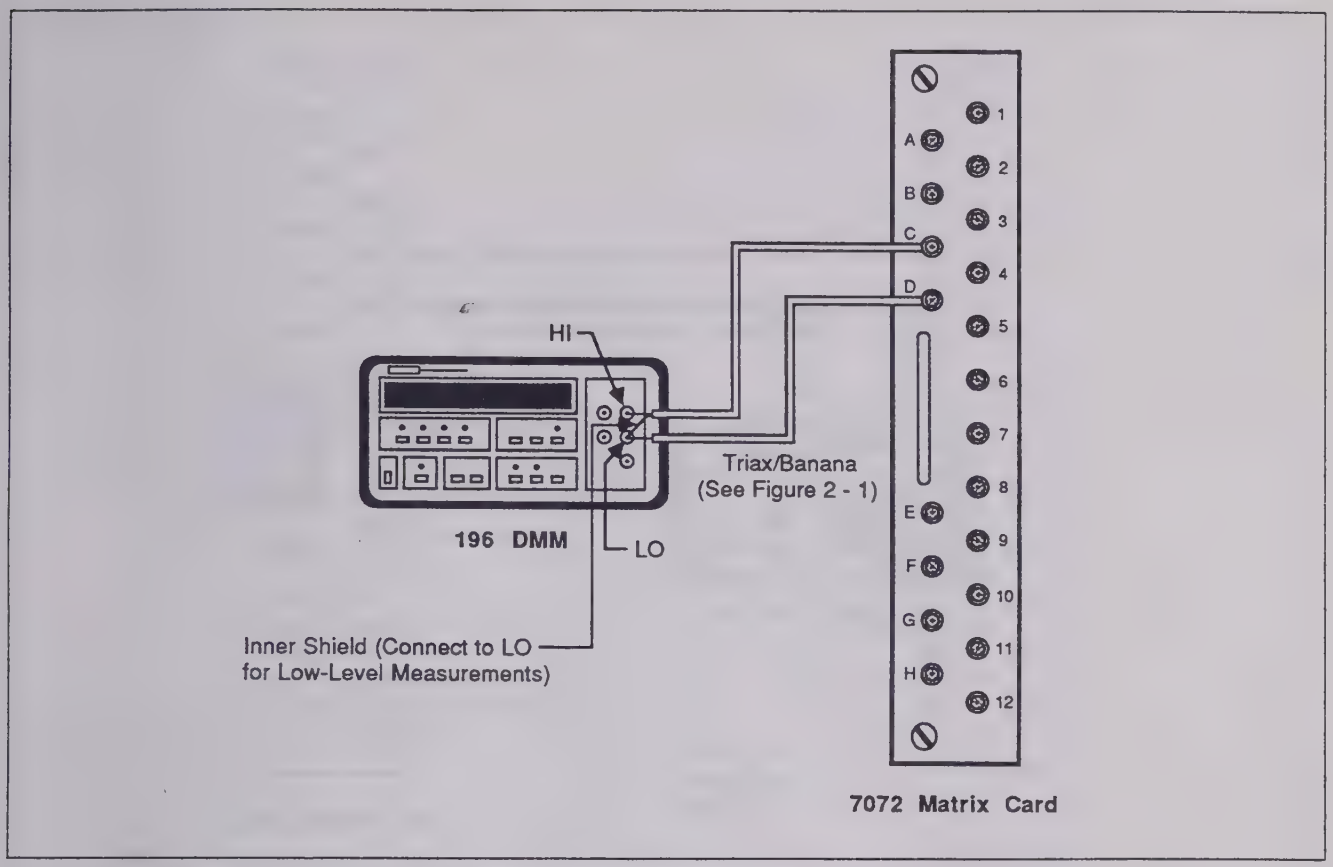


Figure 2-7. Model 196 DMM Connections

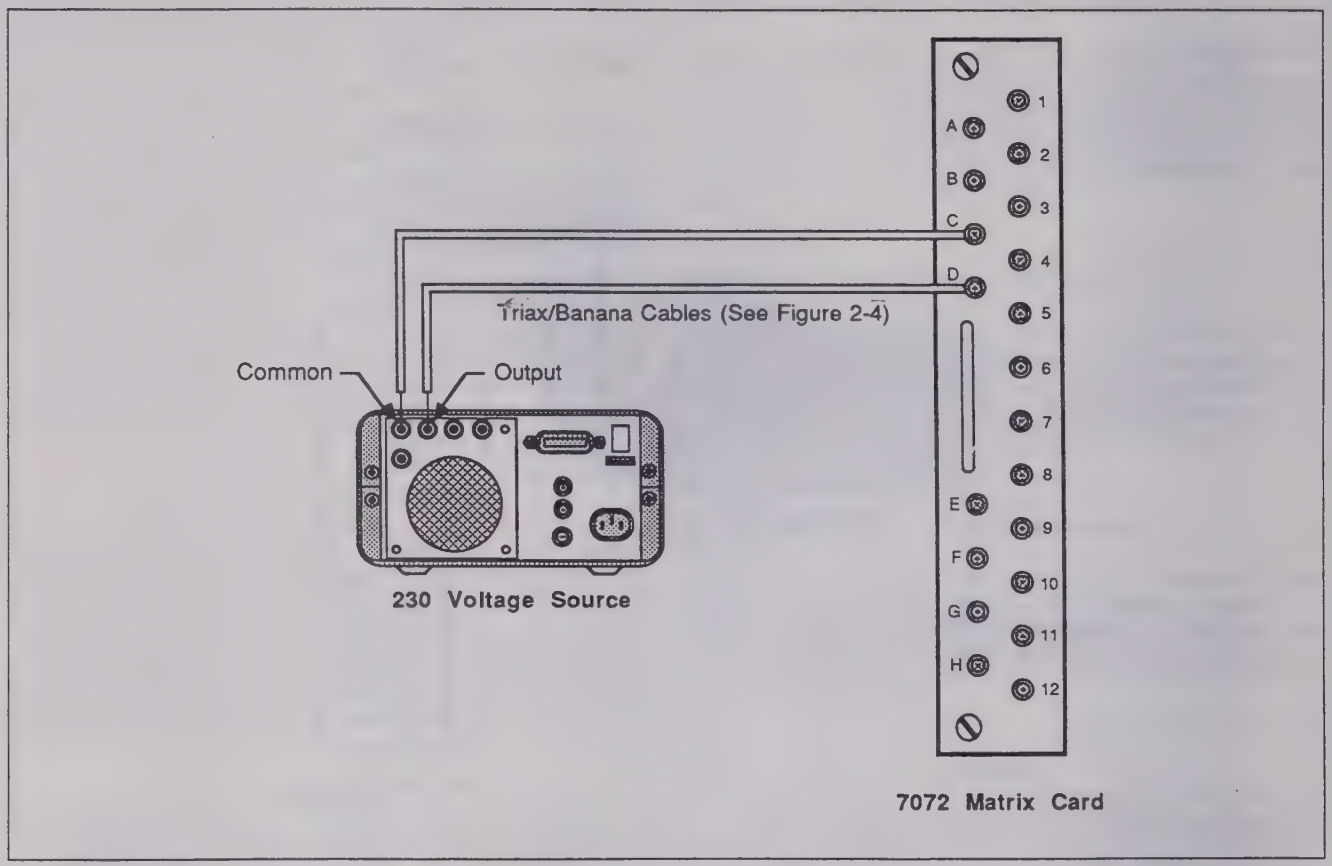


Figure 2-8. Model 230 Voltage Source Connections

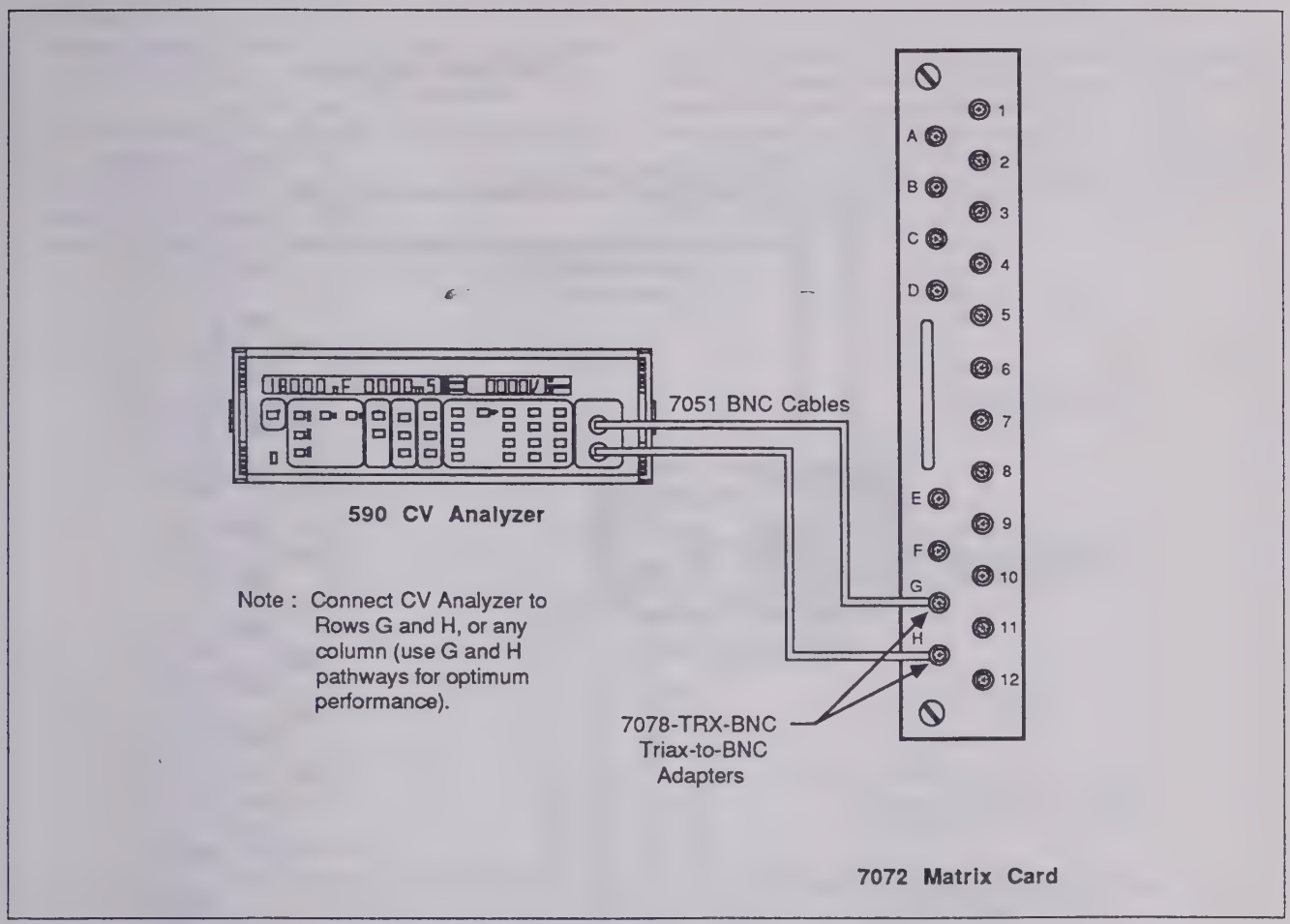


Figure 2-9. Model 590 CV Analyzer Connections

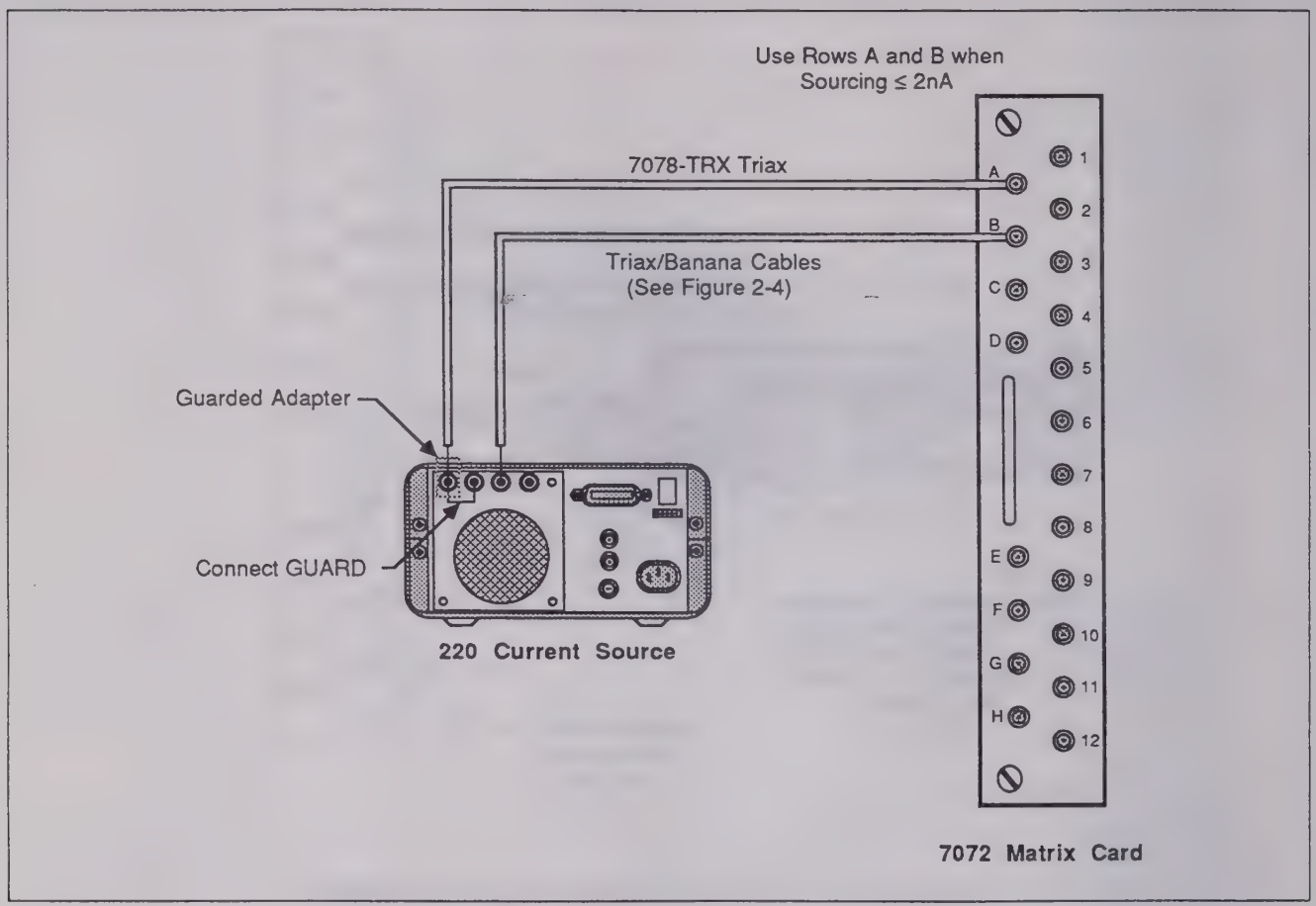


Figure 2-10. Model 220 Current Source Connections

1. Connect the Model 6167 adapter to the Model 220 OUTPUT jack.
2. Connect a Model 7078-TRX-3 or -10 triax cable between the guarded adapter and the desired row of the Model 7072.
3. Connect the Model 220 GUARD output to GUARD INPUT terminal of the adapter.
4. Connect the triax end of a triax/banana cable to the desired row on the Model 7072.
5. Connect the banana plug end of the triax/banana cable to the OUTPUT COMMON jack of the Model 220.

2.5.6 Typical Test Fixture Connections

Typically, one or more test fixtures will be connected to desired columns of the Model 7072. Typically, the test fixtures will be equipped with card-edge connectors with wires soldered to them. In some cases, the test fixture will be equipped with triax connectors; for those types, Keithley Model 7078-TRX-3 or -10 cables can be used, as shown in Figure 2-11.

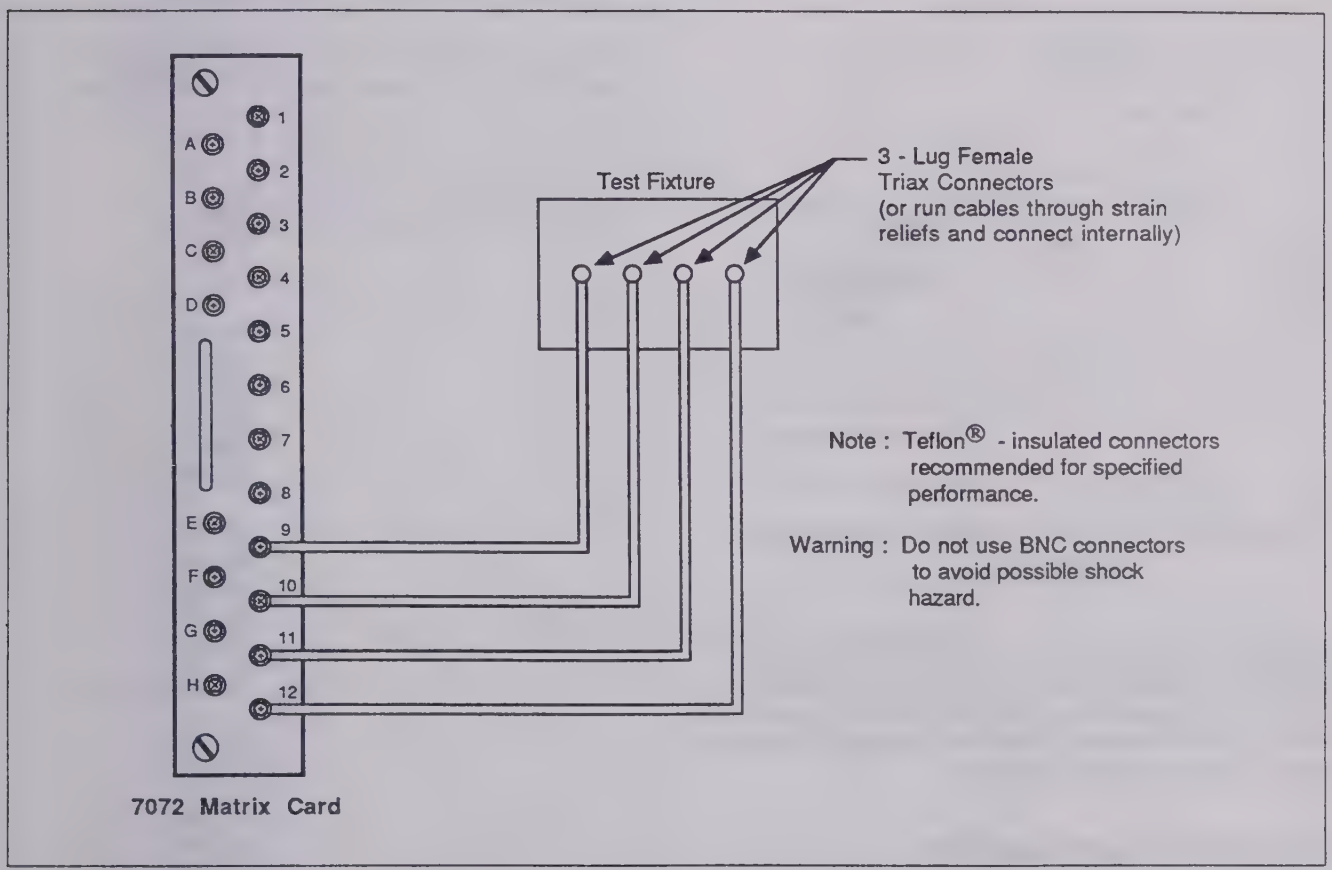


Figure 2-11. Typical Test Fixture Connections

WARNING

Do not use BNC cables and adapters in cases where hazardous voltages from guard sources could be present on the BNC cable shields.

Internally, the test fixture should be wired as shown in the equivalent circuit of Figure 2-12. SIGNAL should be connected to the probe or other device contact points, while GUARD should be carried through as close to the device as possible. If coaxial probes are to be used, connect GUARD to the probe shield if the probe shield is insulated from the fixture shield.

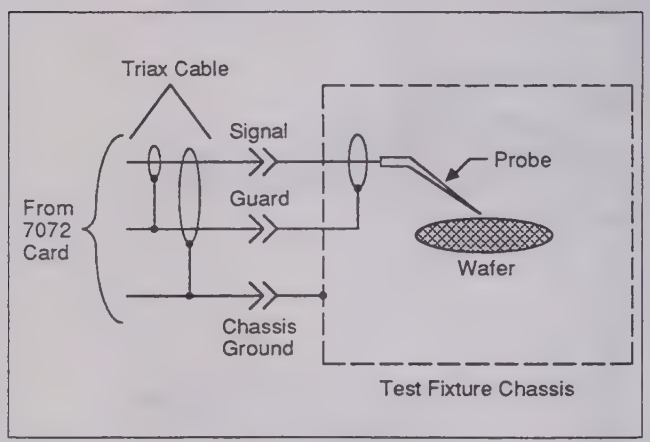


Figure 2-12. Equivalent Circuit of Test Fixture Connections

Usually, the chassis ground terminal of the triax connector will automatically make contact with the fixture shield by virtue of the mounting method. However, ground integrity should be checked to ensure continued protection against hazardous guard voltages.

2.6 MATRIX CONFIGURATION

The following paragraphs discuss the switching matrix of the Model 7072 as well as how to expand the matrix by connecting two or more cards together.

2.6.1 Switching Matrix

As shown in Figure 2-13, the Model 7072 is organized as an 8 X 12 (eight row by 12 column) matrix. The rows are labelled A through H, while the columns on the card are numbered 1 through 12. The actual column number to use when programming depends on the slot and unit number, as summarized in Table 2-3. For example, card column number 2 on a card in slot 5 of unit 1 is accessed as matrix column 62.

Table 2-3. Column Numbering by Slot and Unit

Unit	Slot	Columns (1-12)
1	1	1-12
	2	13-24
	3	25-36
	4	37-48
	5	49-60
	6	61-72
2	1	73-84
	2	85-96
	3	97-108
	4	109-120
	5	121-132
	6	133-144
3	1	145-156
	2	157-168
	3	169-180
	4	181-192
	5	193-204
	6	205-216
4	1	217-228
	2	229-240
	3	241-252
	4	253-264
	5	265-276
	6	277-288
5	1	289-300
	2	301-312
	3	313-324
	4	325-336
	5	337-348
	6	349-360

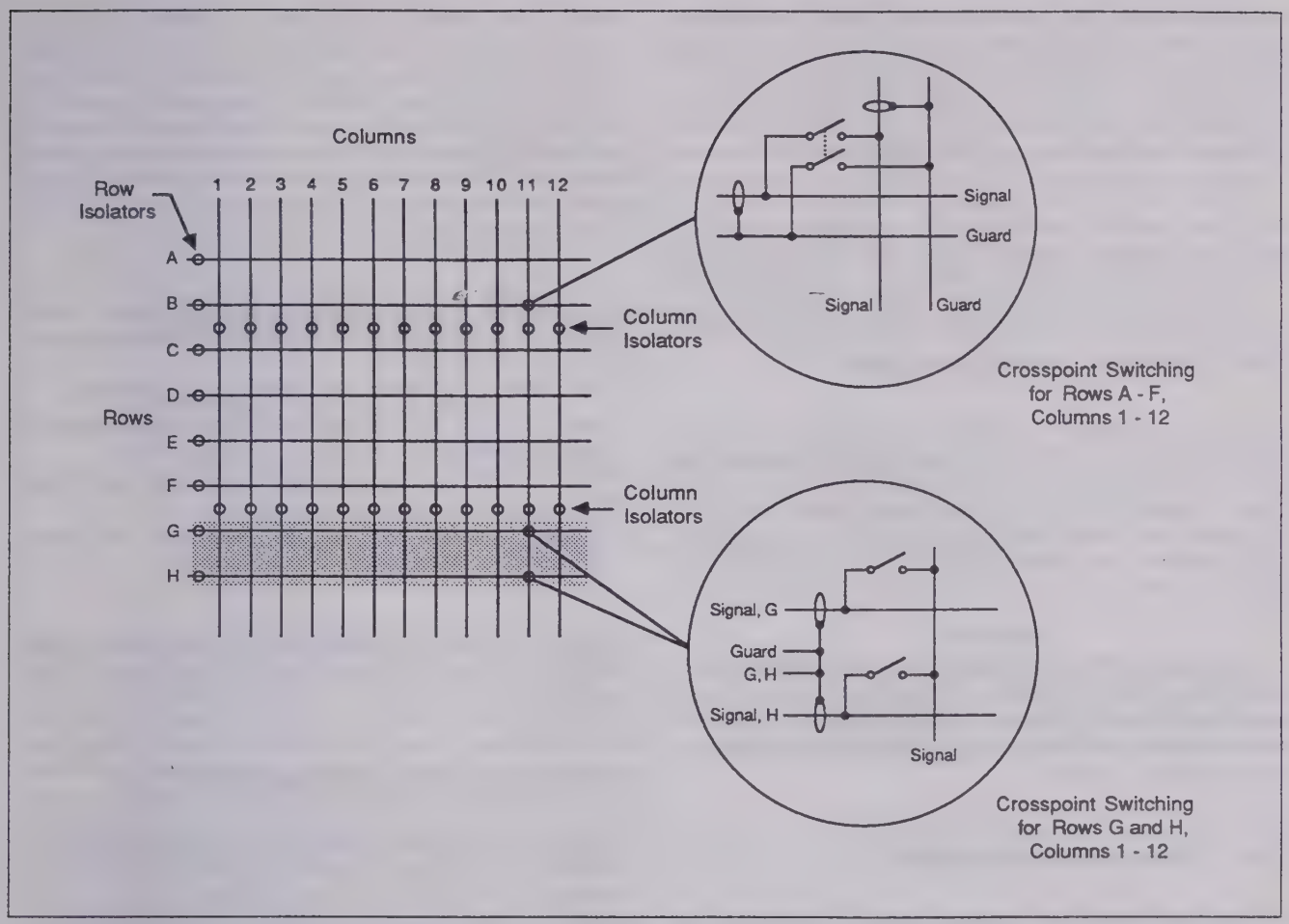


Figure 2-13. Model 7072 Matrix Organization

Each intersecting point in the matrix is called a crosspoint that can be individually closed or opened by programming the Model 707 mainframe. The crosspoints for rows A through F are configured for 2-pole switching, as shown in Figure 2-13. For these rows, SIGNAL and GUARD are switched separately to any of the 12 columns on the card.

The crosspoints for rows G and H use 1-pole switching, with only SIGNAL being switched. The equivalent circuit for this arrangement is also shown in Figure 2-13.

2.6.2 Row and Column Isolators

In order to maintain the integrity of the low-current and CV pathways, isolator relays are incorporated into each column. These isolators are indicated as small circles on the matrix diagram of Figure 2-13. Each relay remains open until a crosspoint located in rows C through H is to be closed. In this manner, the general-purpose pathways are isolated from the more critical low-current and CV pathways.

In a similar manner, row isolator relays isolate the crosspoint relays from a given row to minimize leakage current and capacitance, and maximize path resistance. The row isolator relay closes when any crosspoint relay associated with that row is closed.

2.6.3 Pathway Considerations

As discussed previously, the eight rows on the matrix card are designed for different purposes. Rows A and B are designated low-current rows, rows C through F are general purpose rows, and rows G and H are CV rows.

Many of the specifications for the card differ among row types. For example, the offset current for the low-current rows is <1pA, but the general purpose and CV rows have a higher offset current of 20pA. Thus, A and B would be the rows of choice for low-current measurements. Also, the path isolation for rows A and B is an order of magnitude higher than that the other rows ($10^{13}\Omega$ vs. $10^{12}\Omega$). Again, these two rows would be preferable for very high-impedance measurements.

In summary, the following general rules apply when choosing which rows to use for specific measurements:

- Use rows A and B for low-current measurements.
- Use rows A, B, G, and H for low-capacitance measurements.
- Rows A and B should be used where high path isolation resistance is of primary concern.
- Rows A and B have the largest bandwidth, while rows G and H have the smallest bandwidth.

For more detailed information on these factors, refer to the Model 7072 Specifications located at the front of this manual.

2.6.4 Internal Matrix Expansion

Two to six Model 7072 cards can be connected together within the mainframe to yield an 8 X N matrix, where N depends on the number of cards. Figure 2-14 shows an internally expanded matrix with three cards, resulting in an 8 × 36 (eight row by 36 column) matrix. As summarized in Table 2-3, the actual column number used when programming the unit is determined by the slot.

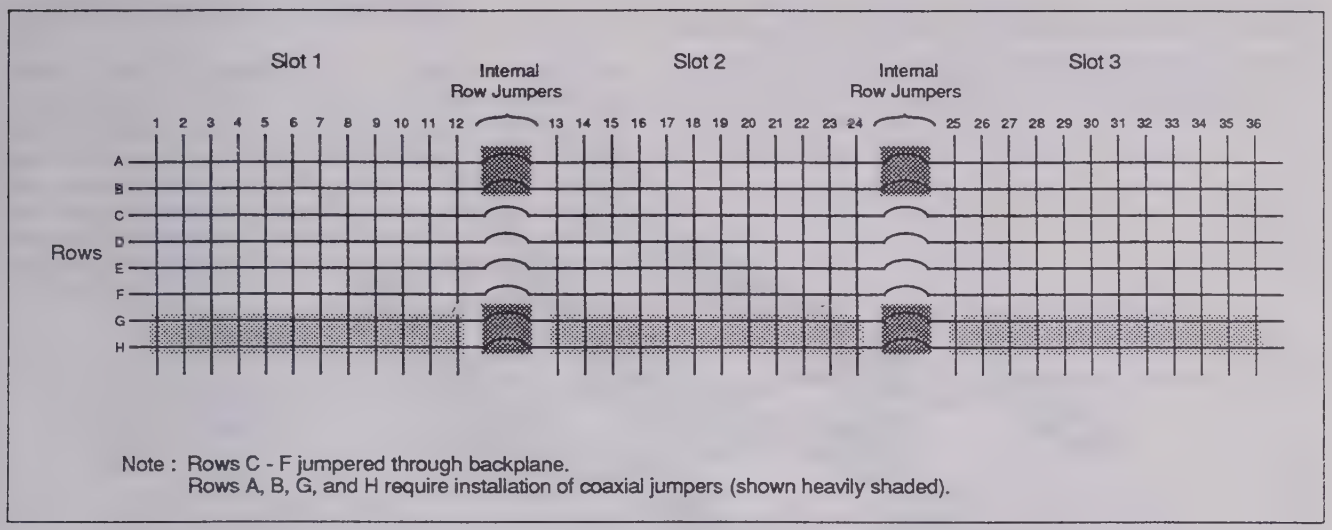

Slot 1
Internal
Row Jumpers
Slot 2
Internal
Row Jumpers
Slot 3
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36
Rows
A
B
C
D
E
F
G
H
Note : Rows C - F jumpered through backplane.
Rows A, B, G, and H require installation of coaxial jumpers (shown heavily shaded).

Figure 2-14. Connecting Three Cards for 8 × 36 Matrix

Rows C through F are automatically connected together through the backplane of the mainframe. The mainframe can be configured for two sets of three cards each by removing jumpers from the backplane of the mainframe; see Section 3 of the Model 707 Instruction Manual for details on removing the jumpers. With the row jumpers removed, rows C through F of Model 7072 cards in slots 1 through 3 are connected, and rows C through F of Model 7072 cards in slots 4 through 6 are connected together.

Because of more critical signal paths, rows A, B, G, and H are not jumpered through the backplane. Instead, you must install the supplied coaxial jumpers between appropriate connectors on Model 7072 cards (for critical signal paths, rows can be isolated from other cards by not installing these cables). Each card has two SMB coaxial connectors for each row, allowing daisy chaining of card rows. These connectors can be reached by lifting the access door on the top of the mainframe; it is not necessary to remove cards to install the jumpers. Figure 2-15 shows an edge-on view of the jumper connectors with row numbers marked for convenience. Figure 2-16 demonstrates how three cards can be daisy chained together using the coaxial jumpers.

WARNING
The SMB coaxial shields are at guard potential. To avoid a possible shock hazard, always disconnect all cables from the row and column jacks before removing or installing jumpers.

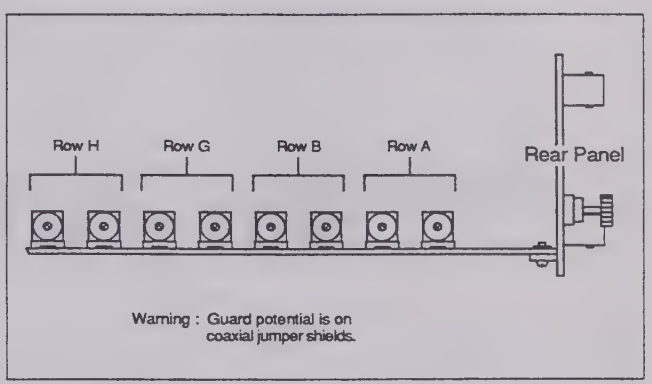


Figure 2-15. Jumper Connector Locations

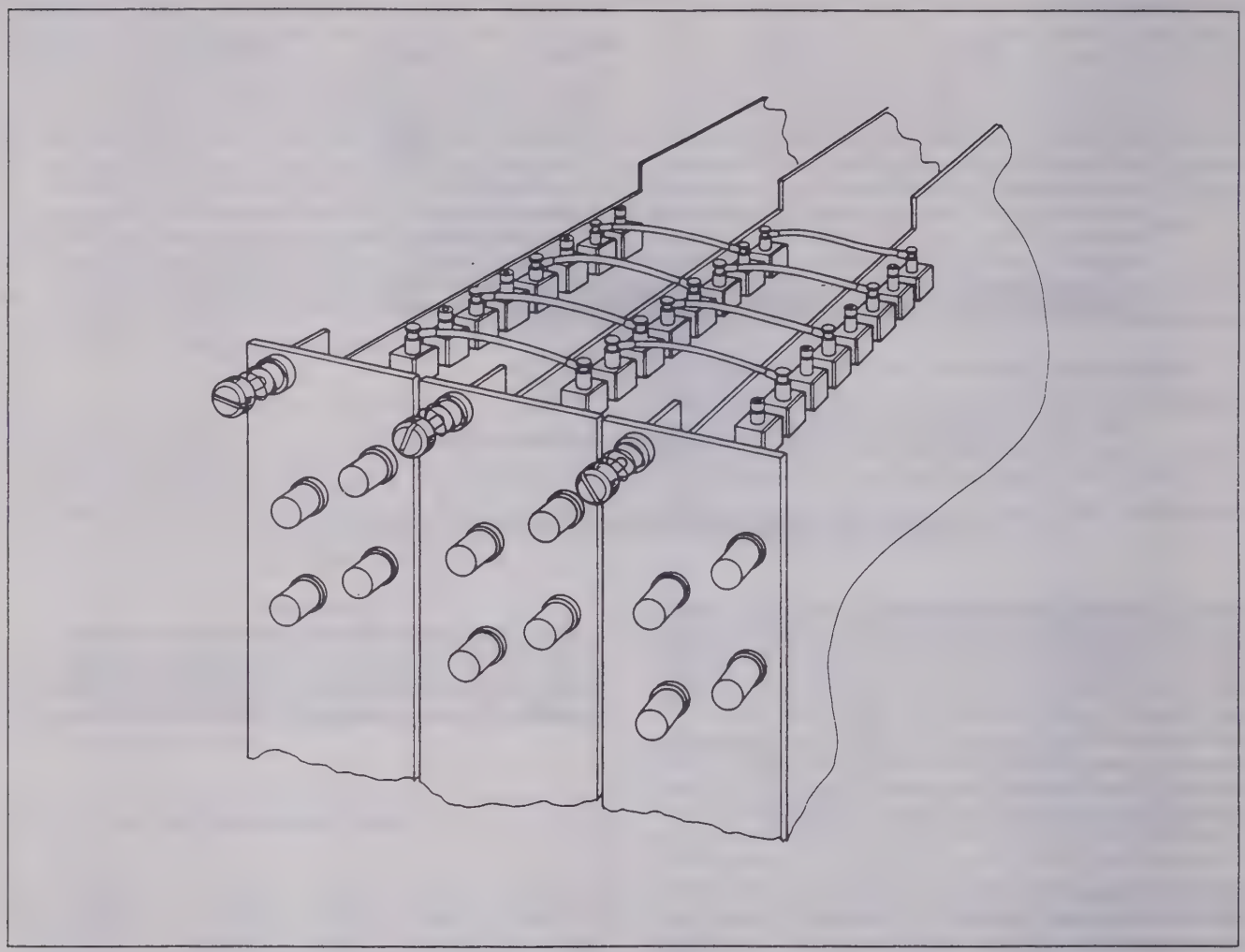


Figure 2-16. Three Cards in Daisy Chain Configuration

2.6.5 External Matrix Expansion

External jumper cables must be used to expand the number of rows in the matrix, or to connect between columns of cards installed in different mainframes. An example of such an expanded matrix is shown in Figure 2-17. Here, six cards are configured as a 16 × 36 matrix. Since the rows are internally jumpered, only columns must be jumpered externally in this configuration. Note that the backplane jumpers must be removed to separate the cards into two groups.

Triax tee adapters (Model 7078-TRX-T) can be used to provide daisy chain capability between the triax input connectors. Figure 2-18 shows a typical arrangement between two Model 7072 cards. Ideally, custom-length triax cables should be used to avoid the cable "jungle" that would occur with longer, standard-length cables.

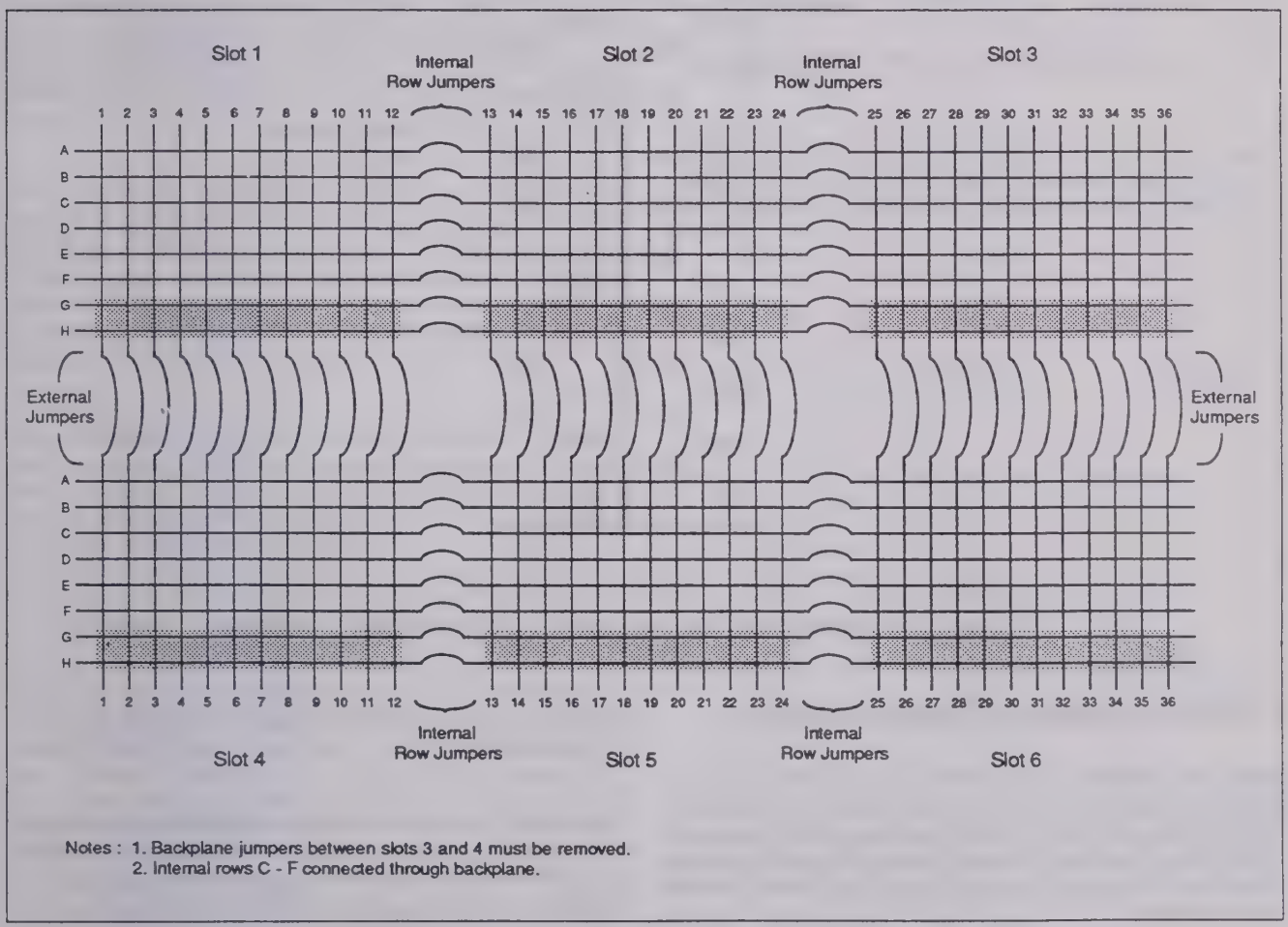

Slot 1
Internal Row Jumpers
Slot 2
Internal Row Jumpers
Slot 3
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36
A
B
C
D
E
F
G
H
External Jumpers
External Jumpers
Slot 4
Internal Row Jumpers
Slot 5
Internal Row Jumpers
Slot 6
Notes : 1. Backplane jumpers between slots 3 and 4 must be removed.
2. Internal rows C - F connected through backplane.

Figure 2-17. 16 × 36 Matrix Constructed by External Jumpering

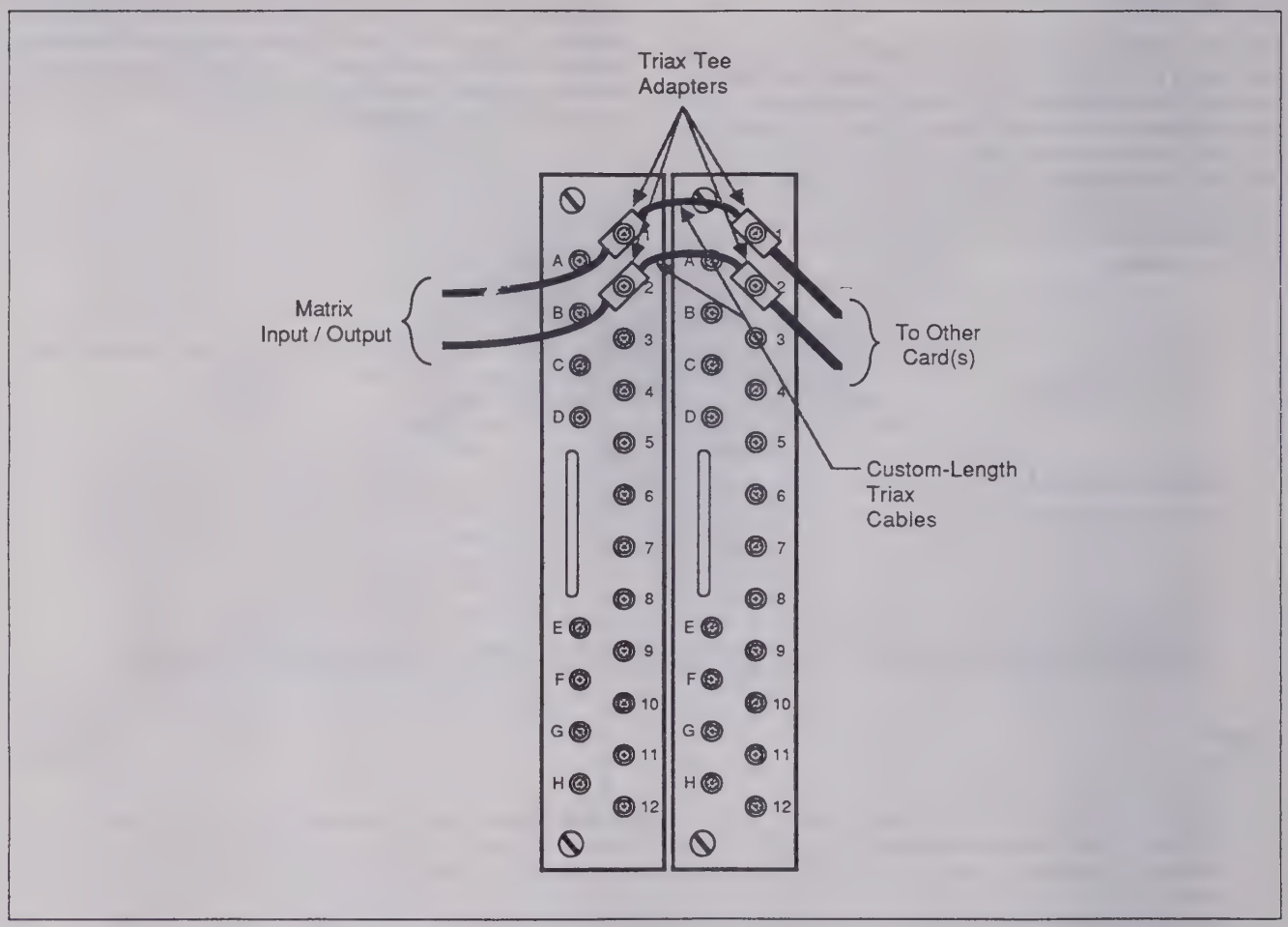


Figure 2-18. Using Triax Tee Adapters to Daisy Chain Cards

2.7 MEASUREMENT CONSIDERATIONS

Many measurements made with the Model 7072 concern low-level signals. Such measurements are subject to various types of noise that can seriously affect low-level measurement accuracy. The following paragraphs discuss possible noise sources that might affect these measurements.

2.7.1 Magnetic Fields

When a conductor cuts through magnetic lines of force, a very small current is generated. This phenomenon will frequently cause unwanted signals to occur in the test leads of a switching matrix system. If the conductor has sufficient length, even weak magnetic fields like those of the earth can create sufficient signals to affect low-level measurements.

Two ways to reduce these effects are: (1) reduce the lengths of the test leads, and (2) minimize the exposed circuit area. In extreme cases, magnetic shielding may be required. Special metal with high permeability at low flux densities (such as mu metal) are effective at reducing these effects.

Even when the conductor is stationary, magnetically-induced signals may still be a problem. Fields can be produced by various signals such as the AC power line voltage. Large inductors such as power transformers can generate substantial magnetic fields, so care must be taken to keep the switching and measuring circuits a good distance away from these potential noise sources.

2.7.2 Radio Frequency Interference

RFI (Radio Frequency Interference) is a general term used to describe electromagnetic interference over a wide range of frequencies across the spectrum. Such RFI can be particularly troublesome at low signal levels, but it can also affect measurements at high levels if the problem is of sufficient severity.

RFI can be caused by steady-state sources such as radio or TV signals, or some types of electronic equipment (microprocessors, high speed digital circuits, etc.), or it can result from impulse sources, as in the case of arcing in high-voltage environments. In either case, the effect on the measurement can be considerable if enough of the unwanted signal is present. A common problem is the rectification by semiconductor junctions of RF picked up by leads.

RFI can be minimized in several ways. The most obvious method is to keep the equipment and signal leads as far away from the RFI source as possible. Shielding the signal leads, sources, and measuring instruments will often reduce RFI to an acceptable level. In extreme cases, a specially-constructed screen room may be required to sufficiently attenuate the troublesome signal.

Many instruments incorporate internal filtering that may help to reduce RFI effects in some situations. In some cases, additional external filtering may also be required. Keep in mind, however, that filtering may have detrimental effects on the desired signal.

2.7.3 Ground Loops

When two or more instruments are connected together, care must be taken to avoid unwanted signals caused by ground loops. Ground loops usually occur when sensitive instrumention is connected to other instrumentation with more than one signal return path such as power line ground. As shown in Figure 2-19, the resulting ground loop causes current to flow through the instrument LO signal leads and then back through power line ground. This circulating current develops a small but undesirable voltage between the LO terminals of the two instruments. This voltage will be added to the source voltage, affecting the accuracy of the measurement.

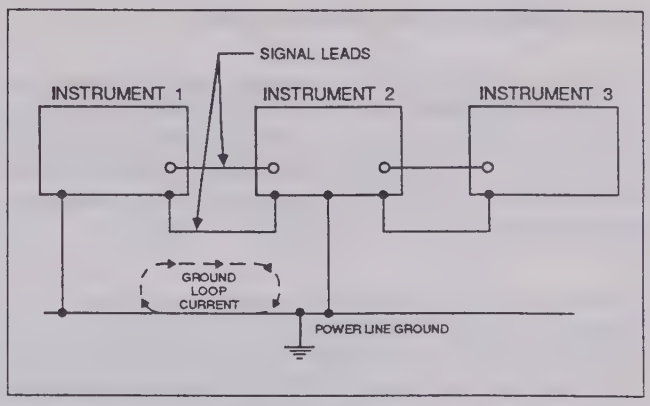


Figure 2-19. Power Line Ground Loops

Figure 2-20 shows how to connect several instruments together to eliminate this type of ground loop problem. Here, only one instrument is connected to power line ground.

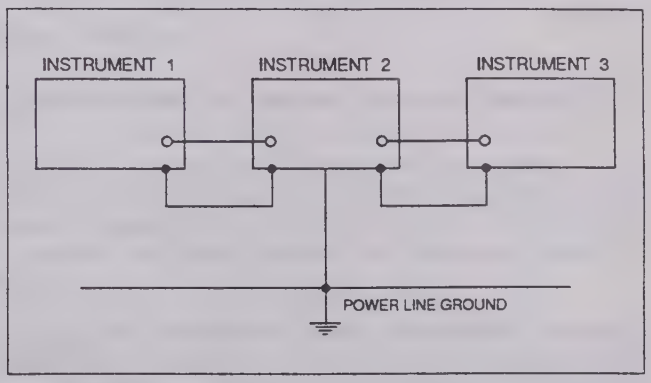


Figure 2-20. Eliminating Ground Loops

Ground loops are not normally a problem with instruments having isolated LO terminals. However, all instruments in the test setup may not be designed in this manner. When in doubt, consult the manual for all instrumentation in the test setup.

2.7.4 Keeping Connectors Clean

As is the case with any high-resistance device, the integrity of triaxial and other connectors can be damaged if they are not handled properly. If the connector insulation becomes contaminated, the insulation resistance will be substantially reduced, affecting high-impedance measurement paths.

Oils and salts from the skin can contaminate connector insulators, reducing their resistance. Also, contaminants present in the air can be deposited on the insulator surface. To avoid these problems, never touch the connector insulating material. In addition, the matrix card should be used only in clean, dry environments to avoid contamination.

If the connector insulators should become contaminated, either by inadvertent touching, or from air-borne deposits, they can be cleaned with a cotton swab dipped in clean methanol. After thorough cleaning, they should be allowed to dry for several hours in a low-humidity environment before use, or they can be dried more quickly using dry nitrogen.

2.7.5 Noise Currents Caused by Cable Flexing

Noise currents can be generated by bending or flexing coaxial or triaxial cables. Such currents, which are known as triboelectric currents, are generated by charges created between a conductor and insulator caused by friction.

Low-noise cable can be used to minimize these effects. Such cable has a special graphite coating under the shield to provide lubrication and to provide a conduction path to equalize charges.

Even low-noise cable generates some noise currents when flexed or subjected to vibration. To minimize these effects, keep the cables as short as possible, and do not subject them to temperature variations that could cause expansion or contraction. Tie down offending cables securely to avoid movement, and isolate or remove vibration sources such as motors or pumps.

2.7.6 Shielding

Proper shielding of all unguarded signal paths and devices under test is important to minimize noise pickup in virtually any switching matrix system. Otherwise, interference from such noise sources as line frequency and RF fields can seriously corrupt a measurement.

In order for shielding to be effective, the shield surrounding the HI signal path should be connected to signal LO (or chassis ground for instruments without isolated LO terminals). Since most Model 7072 matrix applications call for separately switching LO, a separate connection from LO to the cable shield at the source or measurement end must be provided, as in the example of Figure 2-21. Here, we are using the GUARD path of the Model 7072 to carry the shield out to the device under test. Needless to say, this arrangement should not be used with guarding, as GUARD and LO should not be connected together.

WARNING
Hazardous voltage may be present if LO on any instrument is floated above ground potential.

If the device under test is to be shielded, the shield should be should be connected to the LO terminal. If you are using the GUARD connection as shield, care should be taken to insulate the outer ring of the triaxial connector mounted on the test fixture from the test fixture itself. Otherwise, LO will be connected to chassis ground, possibly resulting in a ground loop. An alternative is to use two shields, one mounted within (and insulated from) the other. In this case, the GUARD path would be connected to the inner shield, while the outer shield would be chassis grounded. This arrangement is shown in Figure 2-22. Incidentally, this configuration is also recommended for guarded applications, with the inner shield as guard, and the outer shield acting as a safety shield.

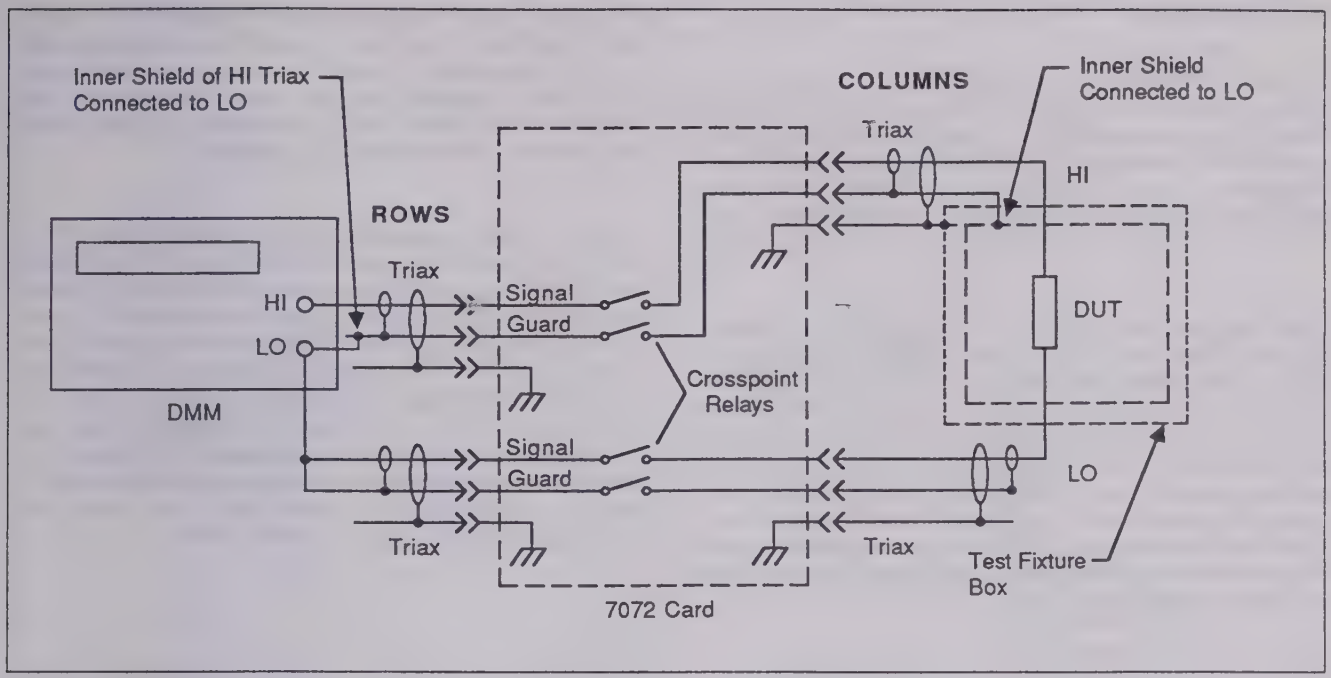


Figure 2-21. Shielding Example

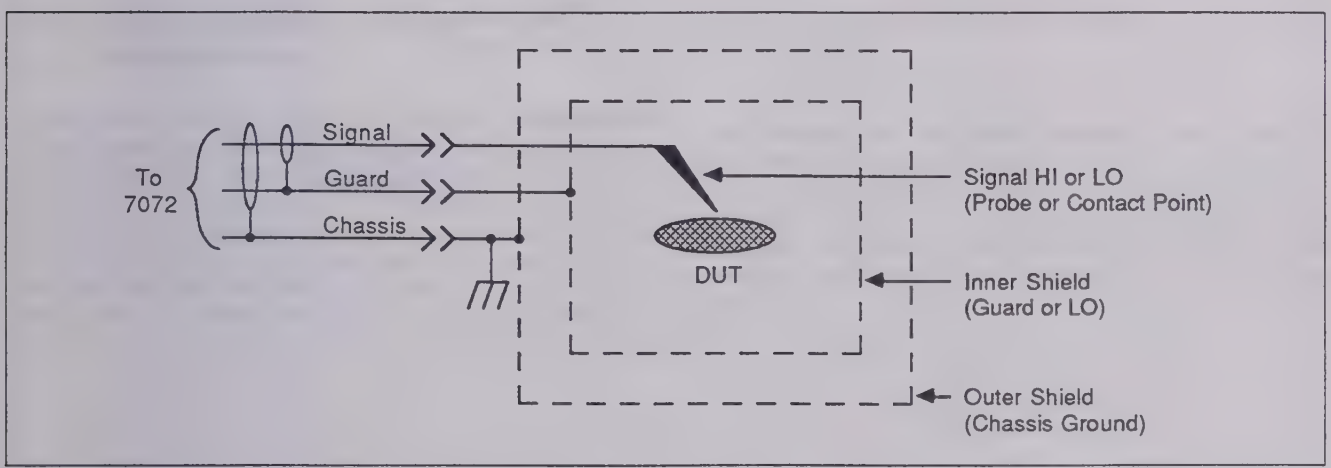


Figure 2-22. Dual Shield Test Fixture

2.7.7 Guarding

Guarding is important in high-impedance circuits where leakage resistance and capacitance could have degrading effects on the measurement. Guarding consists of using a shield surrounding a conductor that is carrying the high-impedance signal. This shield is driven by a low-impedance amplifier to maintain the shield at signal potential. For triaxial cables, the inner shield is used as guard.

Guarding minimizes leakage resistance effects by driving the cable shield with a unity gain amplifier, as shown in Figure 2-23. Since the amplifier has a high input impedance, it minimizes loading on the high-impedance signal lead. Also, the low output impedance ensures that the shield remains at signal potential, so that virtually no leakage current flows through the leakage resistance, R_L. Leakage between inner and outer shields may be considerable, but that leakage is of little consequence because that current is supplied by the buffer amplifier rather than the signal itself.

In a similar manner, guarding also reduces the effective cable capacitance, resulting in much faster measurements on high-impedance circuits. Because any distributed capacitance is charged through the low impedance of the buffer amplifier rather than by the source, settling times are shortened considerably by guarding.

In order to use guarding effectively with the Model 7072, the GUARD path of the matrix card should be connected to the guard output of the sourcing or measuring instrument. Figure 2-24 shows typical connections. Guard should be properly carried through the inner shield to the device under test to be completely effective. The shielded, guarded test fixture arrangement shown in Figure 2-22 is recommended for safety purposes (guard voltage may be hazardous with some instruments). With most instruments, special adapters or cables may be required to connect guard to the inner shield, and at the same time route signal LO through a separate cable.

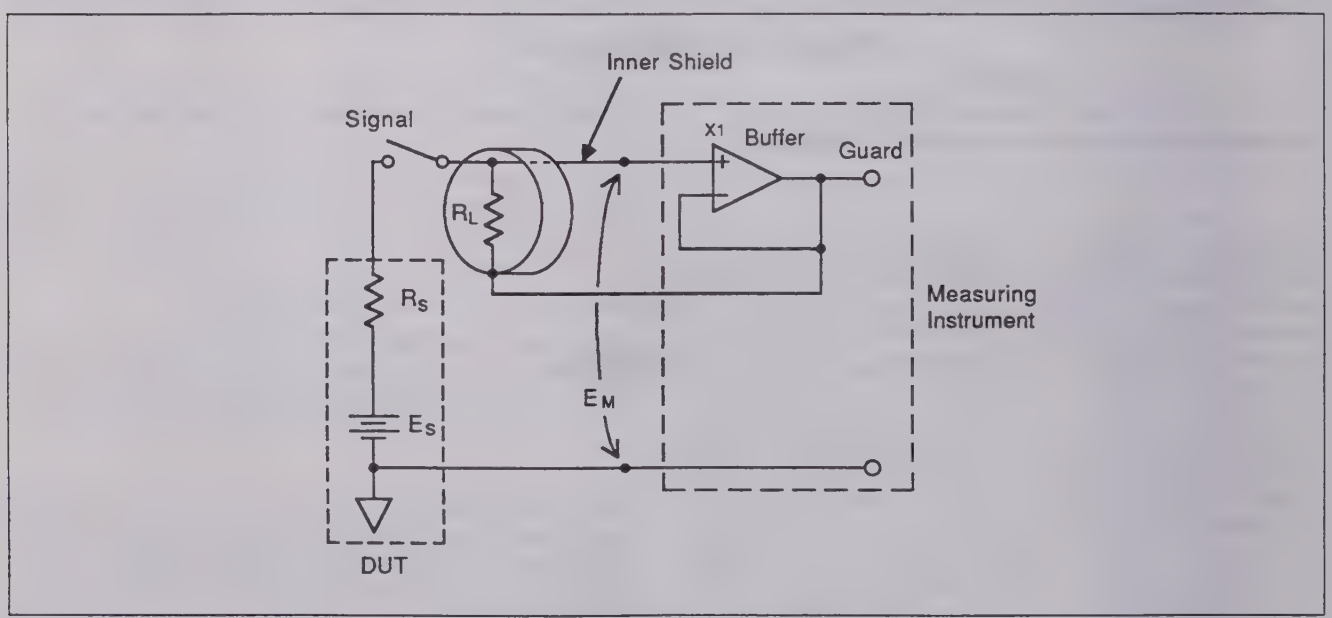


Figure 2-23. Guarded Circuit

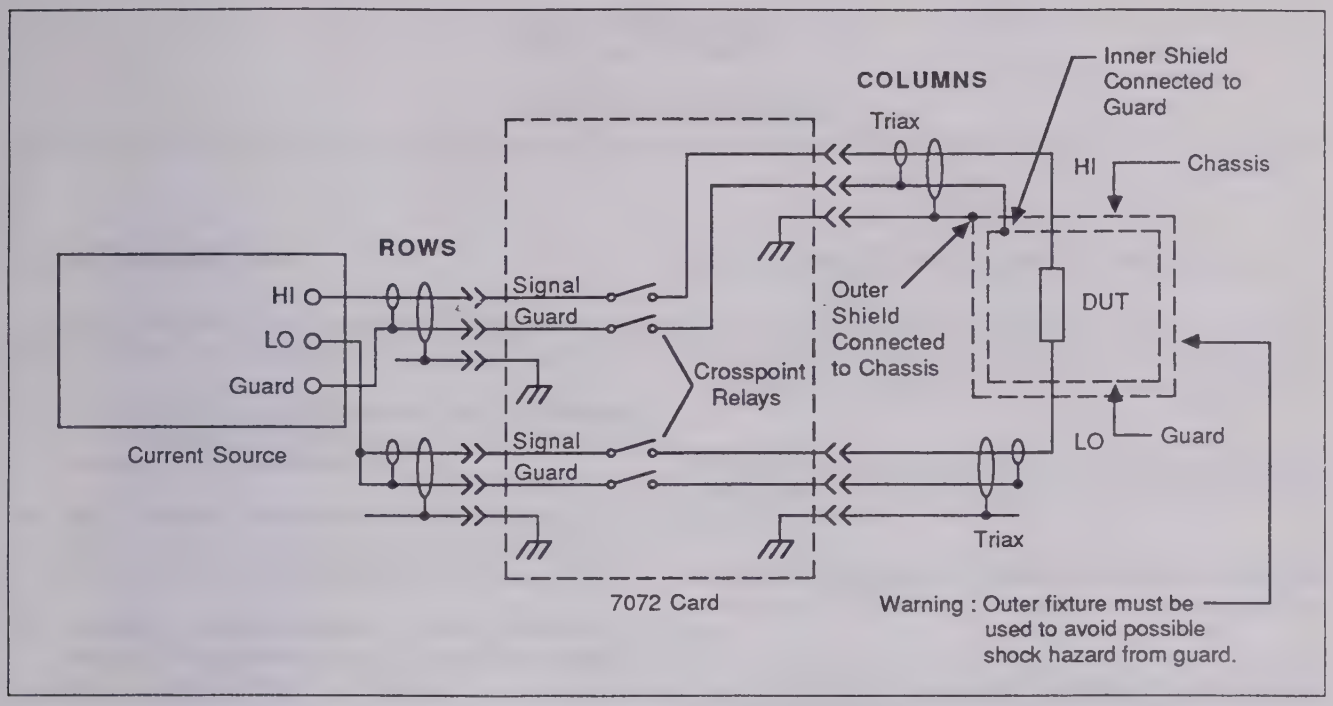


Figure 2-24. Typical Guarded Signal Connections

2.7.8 Matrix Expansion Effects on Card Specifications

Specifications such as those given for path isolation and offset current are with a single Model 7072 Card installed in the mainframe. Expanding the matrix by internally or externally connecting two or more Model 7072 Cards together will degrade system performance specifications (other types of cards do not affect the specifications because they use different pathways in the mainframe backplane). The extent depends on how many cards are used, as well as the amount of cabling used to connect them together.

With internal row expansion, isolation among rows is decreased, and offset current is increased, although the isolator relays on the card do help to minimize these effects. With external row or column expansion, isolation and offset current specifications are degraded because of the additional parallel paths and relays present on each signal line.

SECTION 3
Applications

3.1 INTRODUCTION

This section covers typical applications for the Model 7072 Semiconductor Matrix card and is organized as follows:

3.2 **CV Measurements:** Outlines the test configuration and procedure for making quasistatic and high-frequency CV measurements.

3.3 **Semiconductor Test Matrix:** Details a semiconductor test matrix that can be used to perform a variety of different tests on semiconductors such as FETs.

3.4 **Resistivity Measurements:** Covers methods to measure the resistivity of semiconductor samples using the van der Pauw method.

3.5 **Semiconductor Parameter Analysis:** Discusses using the Model 7072 in conjunction with an HP 4145B Semiconductor Parameter Analyzer.

3.2 CV MEASUREMENTS

The Model 7072 can be used in conjunction the Keithley Model 590 CV Analyzer, and the Keithley Model 595 Quasistatic CV Meter to perform quasistatic and high-frequency CV (capacitance vs. voltage) tests on semiconductors. The resulting CV curves can be used to calculate important semiconductor parameters such as doping profile, band bending, and mobile ion concentration.

3.2.1 Stand Alone System Configuration

The stand alone system shown in Figure 3-1 can be used to make CV measurements without the aid of a computer. System components perform the following functions.

Model 590 CV Analyzer: Measures CV data at 100kHz and 1MHz and sends the resulting data to the plotter for graphing.

Model 595 Quasistatic CV Meter: Measures quasistatic CV data and sends the data to the plotter for graphing in real time.

Model 707 Switching Matrix: Controls the semiconductor matrix card to close and open the desired crosspoints at the proper time.

Model 7072 Semiconductor Matrix Card: Switches the signal pathways to the six wafers under test.

HP-GL Plotter: Plots CV and other curves directly from the Models 590 and 595.

3.2.2 Computerized System Configuration

Figure 3-2 shows a computerized version of the CV matrix test system. The addition of a computer allows greater system versatility and easier instrument control. Also, analysis functions such as doping profile and ion concentration can be added to the software to expand CV analysis capabilities.

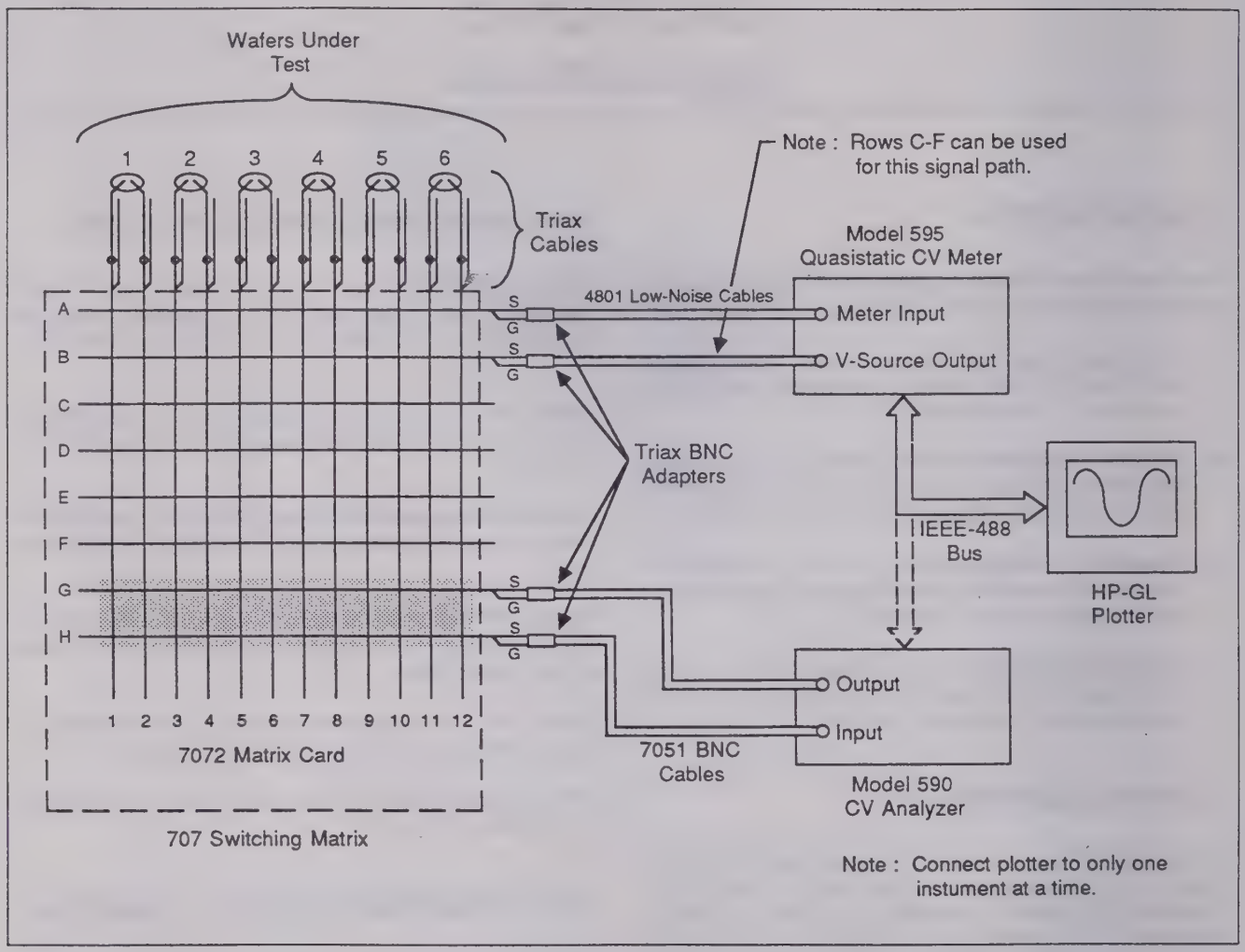


Figure 3-1. Stand Alone CV System Configuration

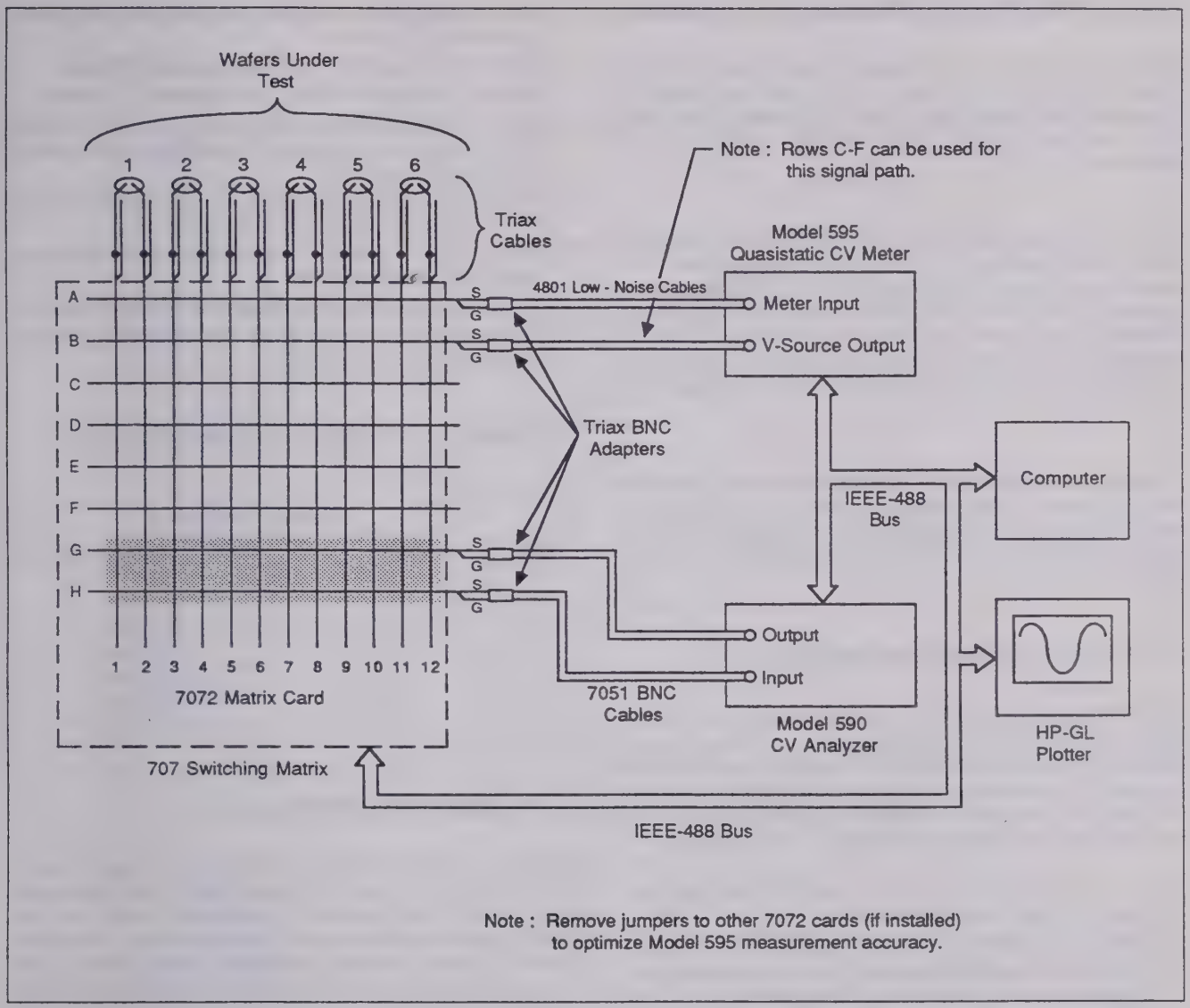


Figure 3-2. Computerized CV System Configuration

3.2.3 Optimizing CV Measurement Accuracy

For accurate CV measurements, each Model 590 CV measurement pathway must be cable corrected using the procedure outlined in the Model 590 Instruction Manual. The pathways to each DUT must be cable corrected separately.

Also, for best quasistatic CV results, the corrected capacitance feature of the Model 595 should be used. Corrected capacitance compensates for any leakage currents present in the cables, switching matrix, or test fixture. However, care must be taken when using corrected capacitance to ensure that the device remains in equilibrium throughout the test sweep to avoid distorting the CV curves.

In order to minimize the effects of the switching network on quasistatic CV measurements, cables to the Model 595 and DUT should be kept as short as possible. Also, the low-current pathways (rows A and B) should be used with the Model 595.

3.2.4 Basic CV Test Procedure

The fundamental CV test procedure is outlined below. Keep in mind that this procedure does not address many considerations and aspects of CV testing, which is fairly complex. The procedure given is for the stand alone system in Figure 3-1. Detailed instrument operating information may be found in the pertinent instruction manuals.

1. Connect the HP-GL plotter to the IEEE-488 bus connector of the Model 595 only.
2. Set up the Model 595 for the expected CV sweep.
3. Close the crosspoints necessary to connect the Model 595 to the device under test, as summarized in Table 3-1. For example, to test device #1, close A1 and B2.
4. Place the probes down on the wafer test dots.
5. Run a quasistatic sweep on the selected device and generate a CV curve.
6. Open the crosspoints that are presently closed.
7. Set up the Model 590 for the expected CV sweep.
8. Close the crosspoints necessary to connect the Model 590 to the device under test. For example, to test device #1, close G1 and H2.
9. Run a high-frequency test sweep on the device to store the CV data in the Model 590 buffer.
10. Disconnect the plotter from the Model 595 and connect it to the Model 590.
11. Generate a plot from the data in the Model 590 buffer.
12. Repeat steps 2 through 11 for the remaining devices, as required.

Table 3-1. CV Test Crosspoint Summary

	Closed Crosspoints	
Wafer #	Quasistatic (595)	High Frequency (590)
1	A1, B2	G1, H2
2	A3, B4	G3, H4
3	A5, B6	G5, H6
4	A7, B8	G7, H8
5	A9, B10	G9, H10
6	A11, B12	G11, H12

3.2.5 Typical CV Curves

Figures 3-3 and 3-4 show typical CV curves as generated by the Models 595 and 590 respectively. The quasistatic curve shows a fair amount of symmetry, while the the high-frequency curve is highly asymmetrical. The asymmetrical nature of the high-frequency curve results from the inability of the minority carriers to follow the high-frequency test signal.

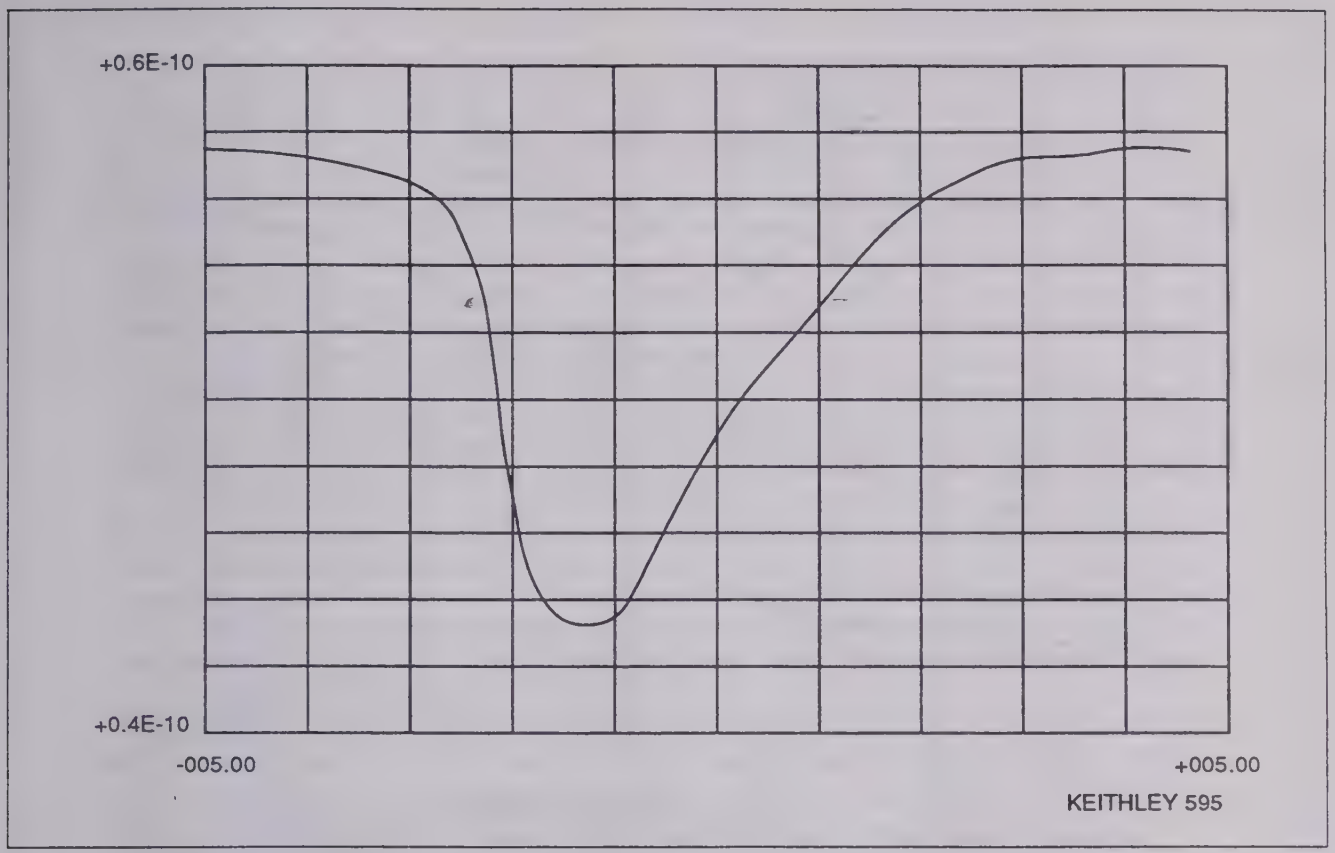


Figure 3-3. Typical Quasistatic CV Curve Generated by Model 595

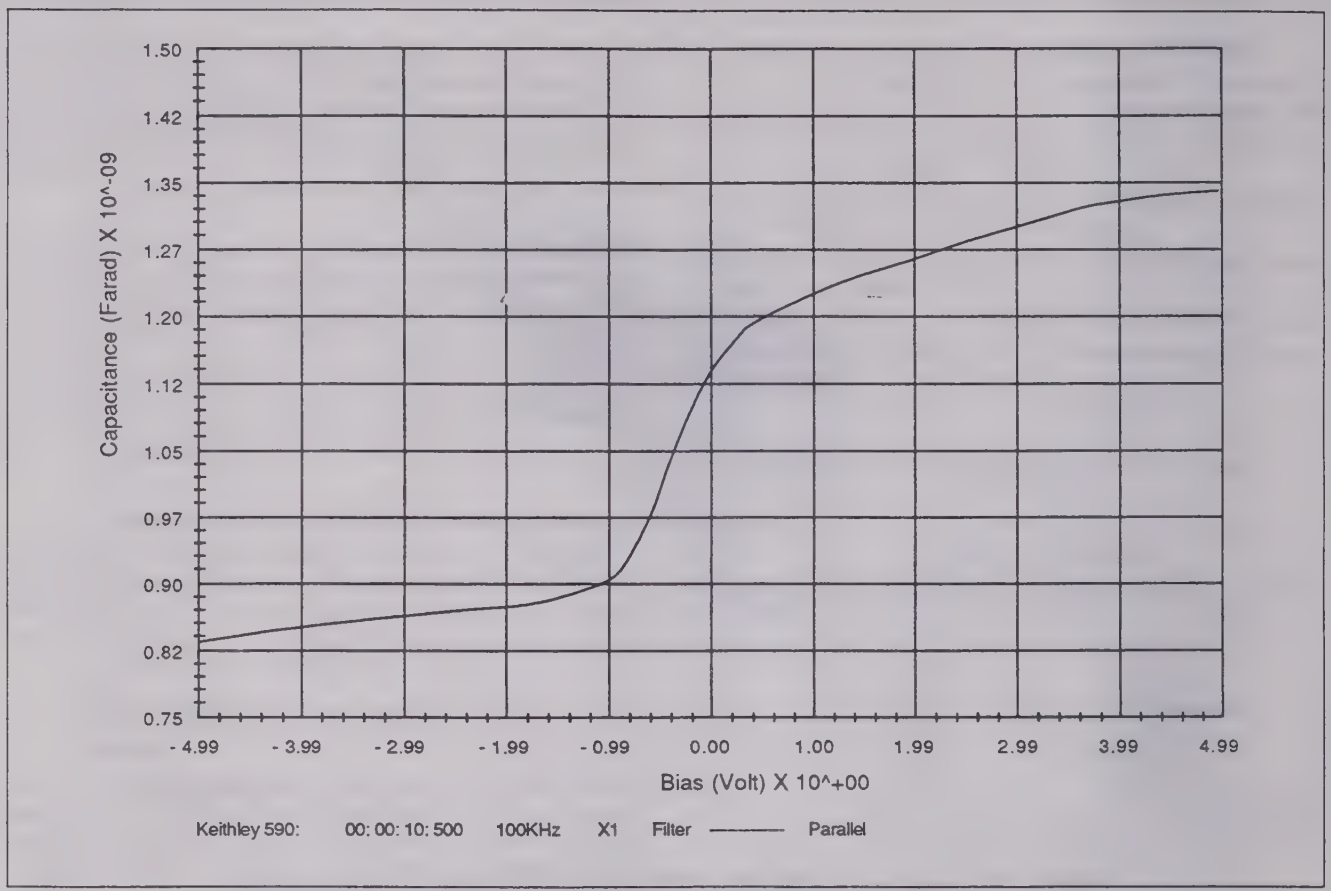


Figure 3-4. Typical High-frequency CV Curve Generated by Model 590

3.3 SEMICONDUCTOR TEST MATRIX

Two important advantages of a matrix switching system are the ability to connect a variety instruments to the device or devices under test, as well as the ability to connect any instrument terminal to any device test node. The following paragraphs discuss a typical semiconductor matrix test system and how to use that system to perform a typical test: common-source characteristic testing of a typical JFET.

3.3.1 System Configuration

Figure 3-5 shows the configuration for a typical multipurpose semiconductor test matrix. Instruments in the system perform the following functions.

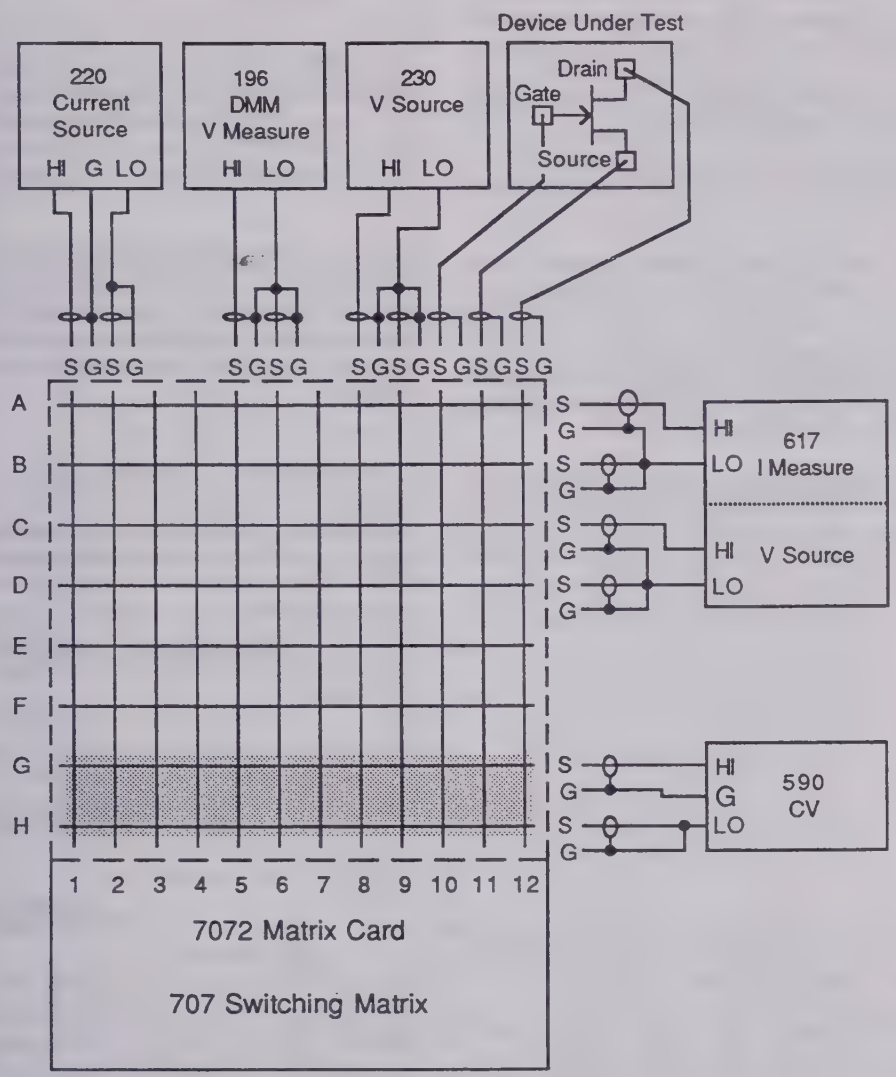


Figure 3-5. Semiconductor Test Matrix

Model 617 Electrometer/Source: Measures current, and also could be used to measure voltages up to ±200VDC. The DC voltage source can supply a maximum of ±100V at currents up to 2mA.

Model 230 Voltage Source: Sources DC voltages up to ±101V at a maximum current of 100mA.

Model 590 CV Analyzer: Adds CV sweep measurement capability to the system.

Model 220 Current Source: Used to source currents up to a maximum of 101mA with a maximum compliance voltage of 105V.

Model 196 DMM: Measure DC voltages in the range of 100nV to 300V. The Model 196 could also be used to measure resistance in certain applications.

Device Under Test: A three-terminal fixture for testing such devices as bipolar transistors and FETs. Additional connections could easily be added to test more complex devices, as required.

3.3.2 Testing Common-Source Characteristic of FETs

The system shown in Figure 3-5 could be used to test a variety of characteristics including I_{GSS}, $I_{D[OFF]}$, $I_{G[ON]}$, I_{DSS}, and $V_{DS[OFF]}$. To demonstrate a practical use for the system, we will show how it can be used to generate common source characteristic curves of a particular JFET.

In order to generate these curves, the instruments must be connected to the JFET under test, as shown in Figure 3-6. The advantage of using the matrix is, of course, that it is a simple matter of closing specific crosspoints. The crosspoints that must be closed are also indicated on the diagram.

To run the test, V_{GS} is set to specific specific values, for example in increments of 0.25V. At each V_{GS} value, the drain-source voltage (V_{DS}) is stepped across the desired range, and the drain current, I_D, is measured at each value of V_{DS} . Once all data are compiled, it is a simple matter to generate the common-source IV curves, an example of which is shown in Figure 3-7. If the system is connected to a computer, the test and graphing could all be done automatically.

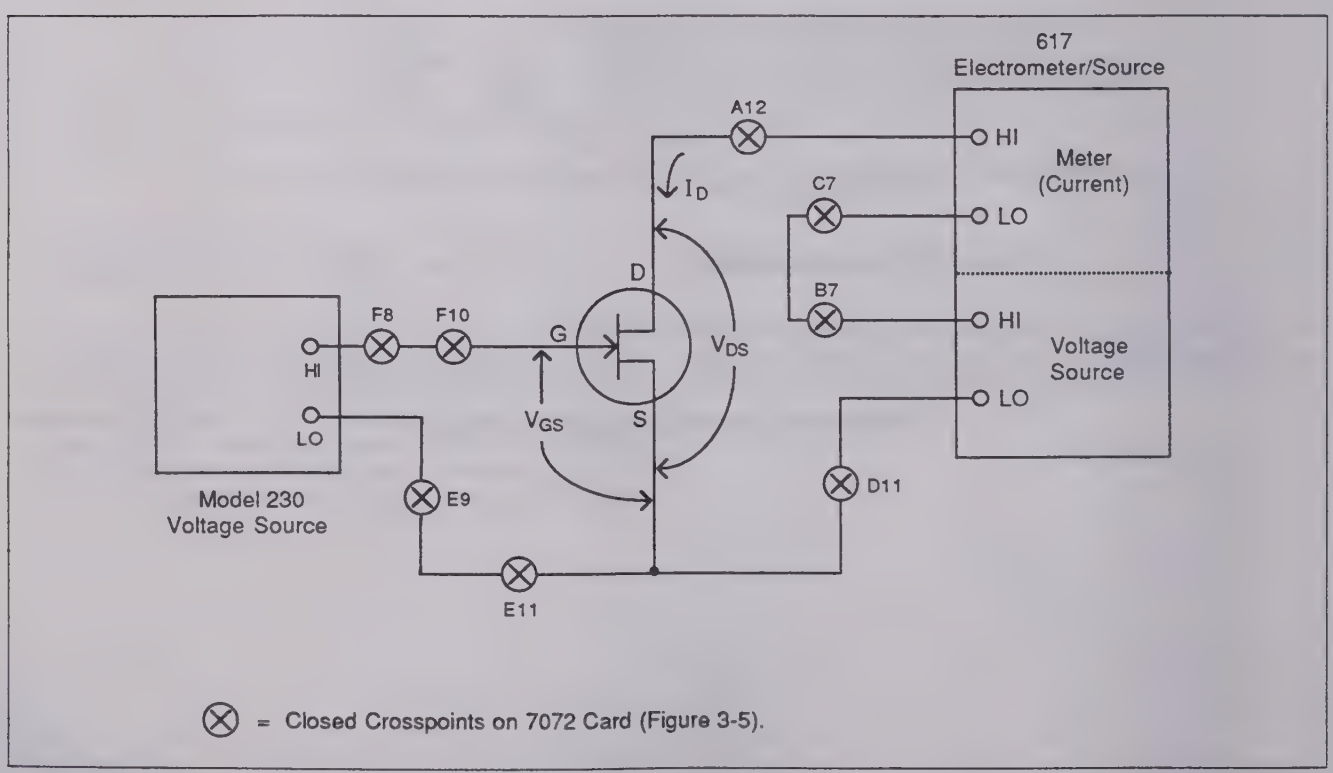


Figure 3-6. System Configuration for Measuring Common-Emitter Characteristics

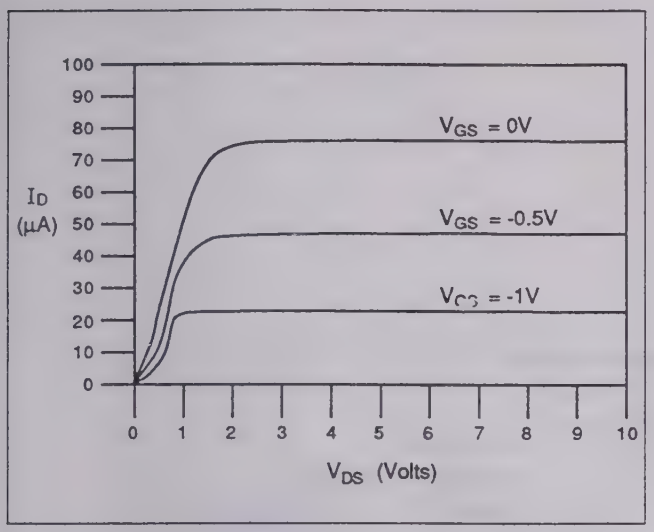


Figure 3-7. Typical Common-Source FET IV Characteristics

3.4 RESISTIVITY MEASUREMENTS

The Model 7072 Semiconductor Matrix card can be used in conjunction with a Model 220 Current Source and a Model 196 DMM to perform resistivity measurements on semiconductors. Such measurements can yield such important information as doping concentration.

3.4.1 Test Configuration

Figure 3-8 shows the basic test configuration to make resistivity measurements on van der Pauw samples. The Model 220 sources current through the samples, while the Model 196 measures the voltage developed across the samples. The matrix card, of course, switches the signal paths as necessary. In order to minimize sample loading, which will reduce accuracy, the Model 196 DMM should be used only on the 300mV or 3V ranges. Also, this configuration is not recommended for resistance measurements above 1MΩ due to the accuracy-degrading effects of DMM loading.

3.4.2 Test Procedure

In order to make van der Pauw resistivity measurements, four terminals of a sample of arbitrary shape are measured. A current (from the Model 220) is applied to two terminals, while the voltage is measured (by the Model 196) across the two opposite terminals, as shown in Figure 3-9. A total of eight such measurements on each sample are required, with each possible terminal and current convention. The resulting voltages are designated V_1 through V_8.

In order to source current into and measure the voltage across the sample, specific crosspoints must be closed. Table 3-2 summarizes the crosspoints to close for each voltage measurement on all three samples from the test configuration shown in Figure 3-8.

3.4.3 Resistivity Calculations

Once the eight voltage measurements are known, the resistivity can be calculated. Two values of resistivity, p_A and p_B are initially computed as follows:

$$p_A = \frac{1.1331\ f_A\ t_S\ (V_2 + V_4 - V_1 - V_3)}{I}$$

$$p_B = \frac{1.1331\ f_B\ t_S\ (V_6 + V_8 - V_5 - V_7)}{I}$$

Where: p_A and p_B are the resitivities in Ω-cm
t_S is the sample thickness in cm
V_1 through V_8 are the voltages measured by the Model 196
I is the current through the sample in amperes
f_A and f_B are geometrical factors based on sample symmetry ($f_A = f_B = 1$ for perfect symmetry).

Once p_A and p_B are known, the average resistivity, p_{AVG}, can be determined as follows:

$$p_{AVG} = \frac{p_A + p_B}{2}$$

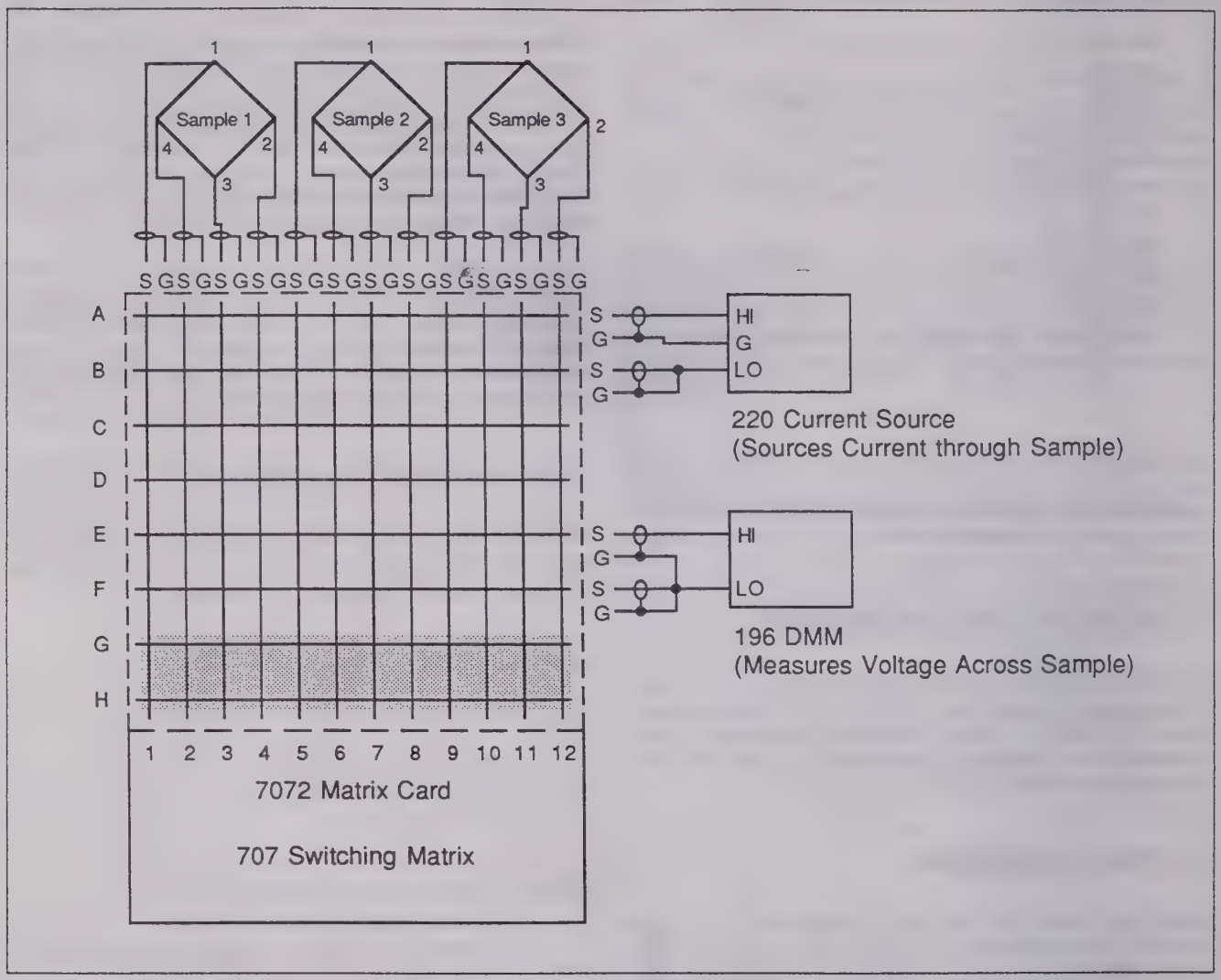


Figure 3-8. Resistivity Test Configuration

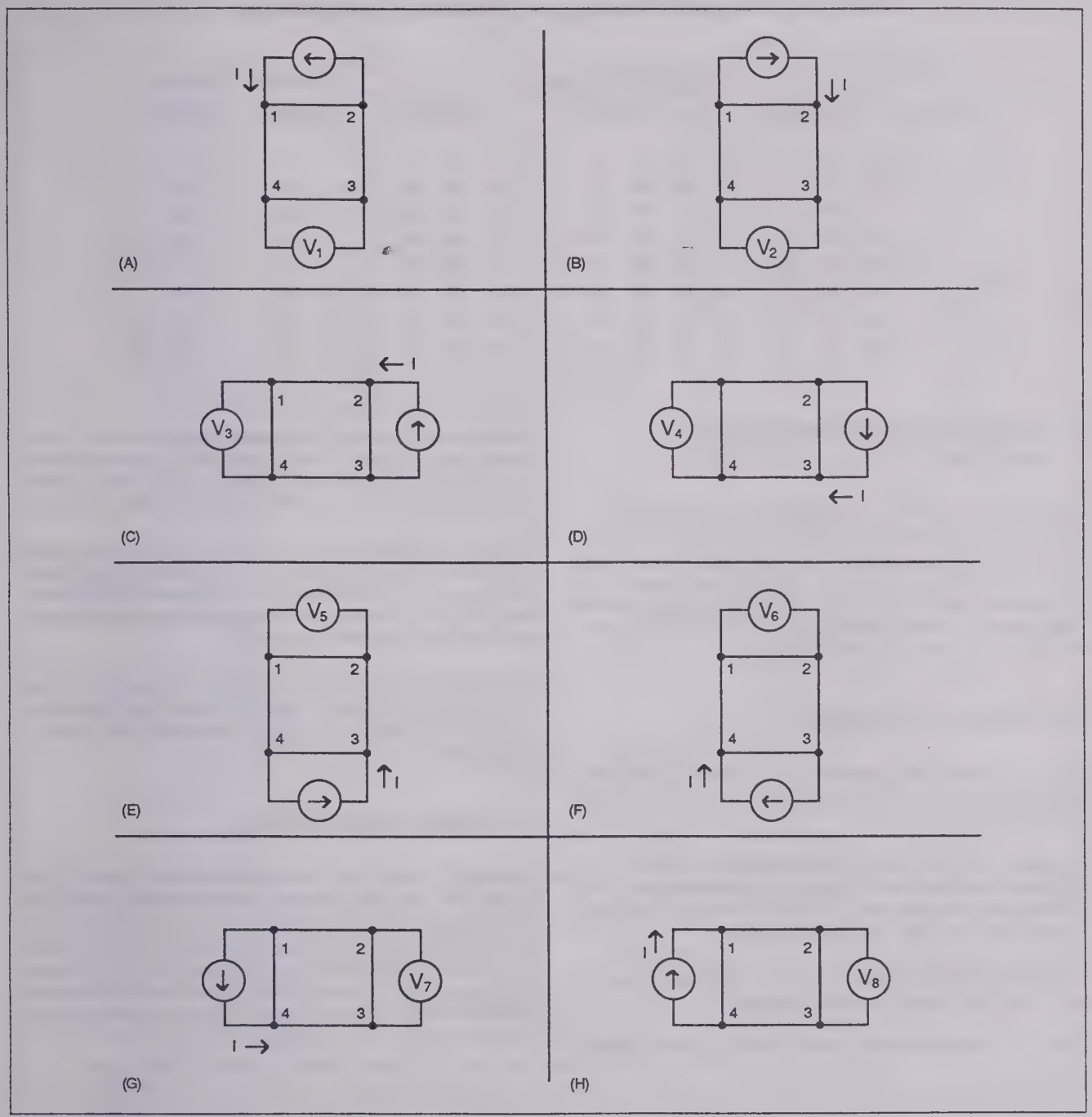


Figure 3-9. Resistivity Measurement Conventions

Table 3-2. Crosspoint Summary for Resistivity Measurements

Voltage	Crosspoints Closed												Current Between	Voltage Between
	Sample #1				Sample #2				Sample #3					
V_1	A1	B4	E3	F2	A5	B9	E7	F6	A9	B12	E11	F10	1-2	3-4
V_2	A4	B1	E3	F2	A8	B5	E7	F6	A12	B9	E11	F10	2-1	3-4
V_3	A4	B3	E2	F1	A8	B7	E6	F5	A12	B11	E10	F9	2-3	4-1
V_4	A3	B4	E2	F1	A7	B8	E6	F5	A11	B12	E10	F9	3-2	4-1
V_5	A3	B2	E1	F4	A7	B6	E5	F8	A11	B10	E9	F12	3-4	1-2
V_6	A2	B3	E1	F4	A6	B7	E5	F8	A10	B11	E9	F12	4-3	1-2
V_7	A2	B1	E4	F3	A6	B5	E8	F7	A10	B9	E12	F11	4-1	2-3
V_8	A1	B2	E4	F3	A5	B6	E8	F7	A9	B10	E12	F11	1-4	2-3

3.5 SEMICONDUCTOR PARAMETER ANALYSIS

One or more Model 7072 Semiconductor Matrix Cards can be used in conjunction with an HP 4145B Semiconductor Parameter Analyzer (SPA) to provide a versatile switching system capable of complete DC characterization of semiconductors. The following paragraphs discuss system configuration, connections using the 7078-CSHP Cable Set, and SPA measurement considerations.

3.5.1 System Configuration

Figure 3-10 shows the general configuration of the SPA switching system. The components of the system perform the following functions:

HP 4145B: Has four SMUs (Source/Measure Units), two voltage sources, and two voltage measurement ports. The unit can automatically run a variety of tests on semiconductors and plot data on a built-in CRT.

Model 707 Switching Matrix: Controls the matrix card to open and close signal paths as required.

Model 7072 Semiconductor Matrix Card: Switches the test pathways to the device under test. In this particular application, three Model 7072 cards provide 36-pin test capability. A total of six cards can be installed in a single mainframe, providing up to 72-pin capability in one mainframe.

System Controller: Controls the SPA and switching matrix with user-written software. Typical controllers for this application are HP 9000 Series 200 or 300 (with HP-IB interface), and IBM PC, AT or compatible computers (equipped with an IEEE-488 interface).

Test Fixture: Provides the interface between the device under test and the matrix card. Typically, the test fixture will be equipped with triax connectors for ease of connections.

3.5.2 Cable Connections

Figure 3-11 shows how to connect the HP 4145B to the Model 7072 using the optional Keithley Model 7078-CSHP Cable Set. The four SMU ports are to be connected with the triax cables (7078-TRX-10), while the two voltage source and voltage measurement ports (Vs and Vm) are to be connected using BNC cables (7051-10) and triax-BNC adapters (7078-TRX-BNC). Typically, the SPA will be connected to the rows, as shown in Figure 3-11.

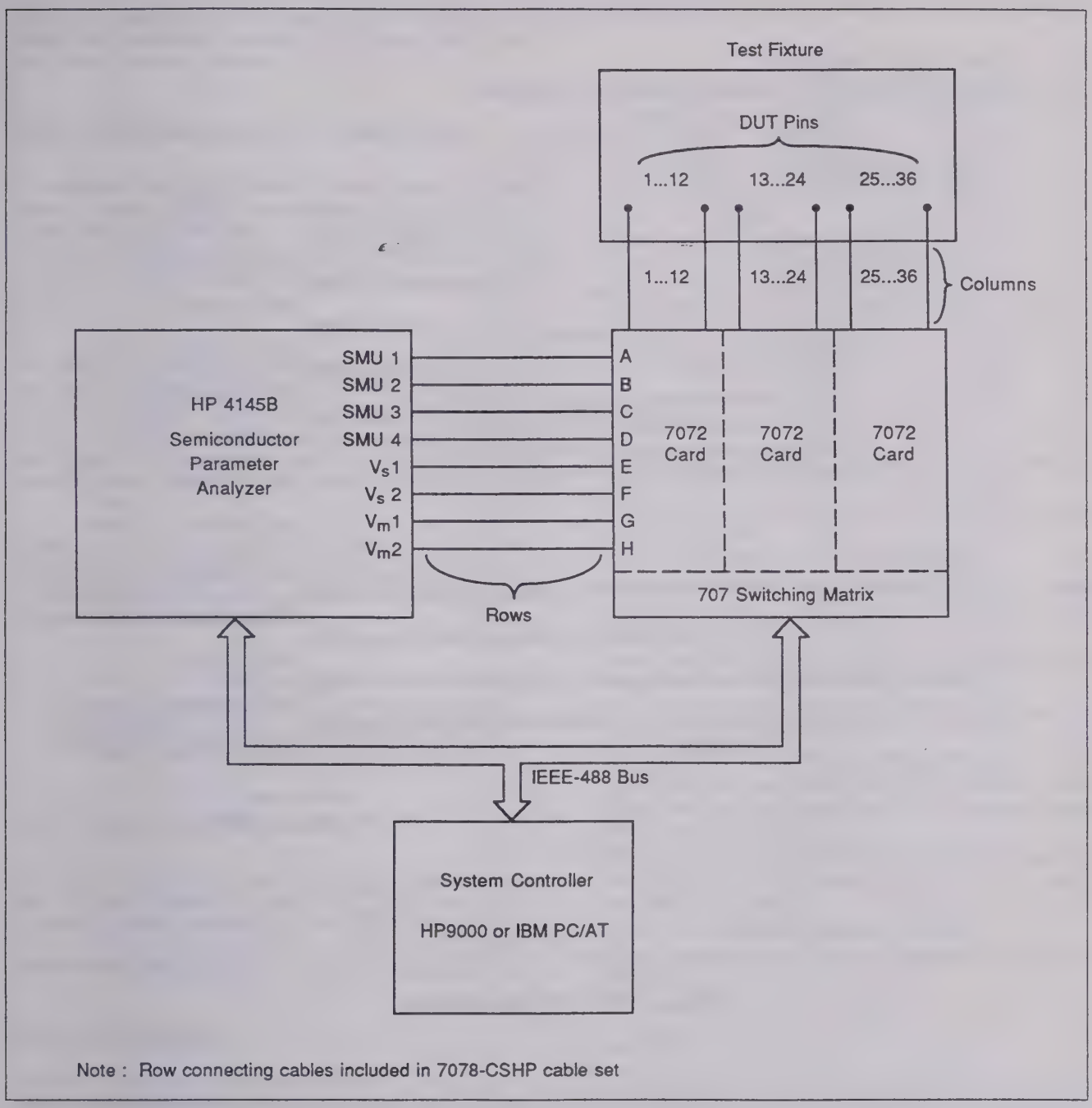


Figure 3-10. Semiconductor Parameter Analysis Switching System

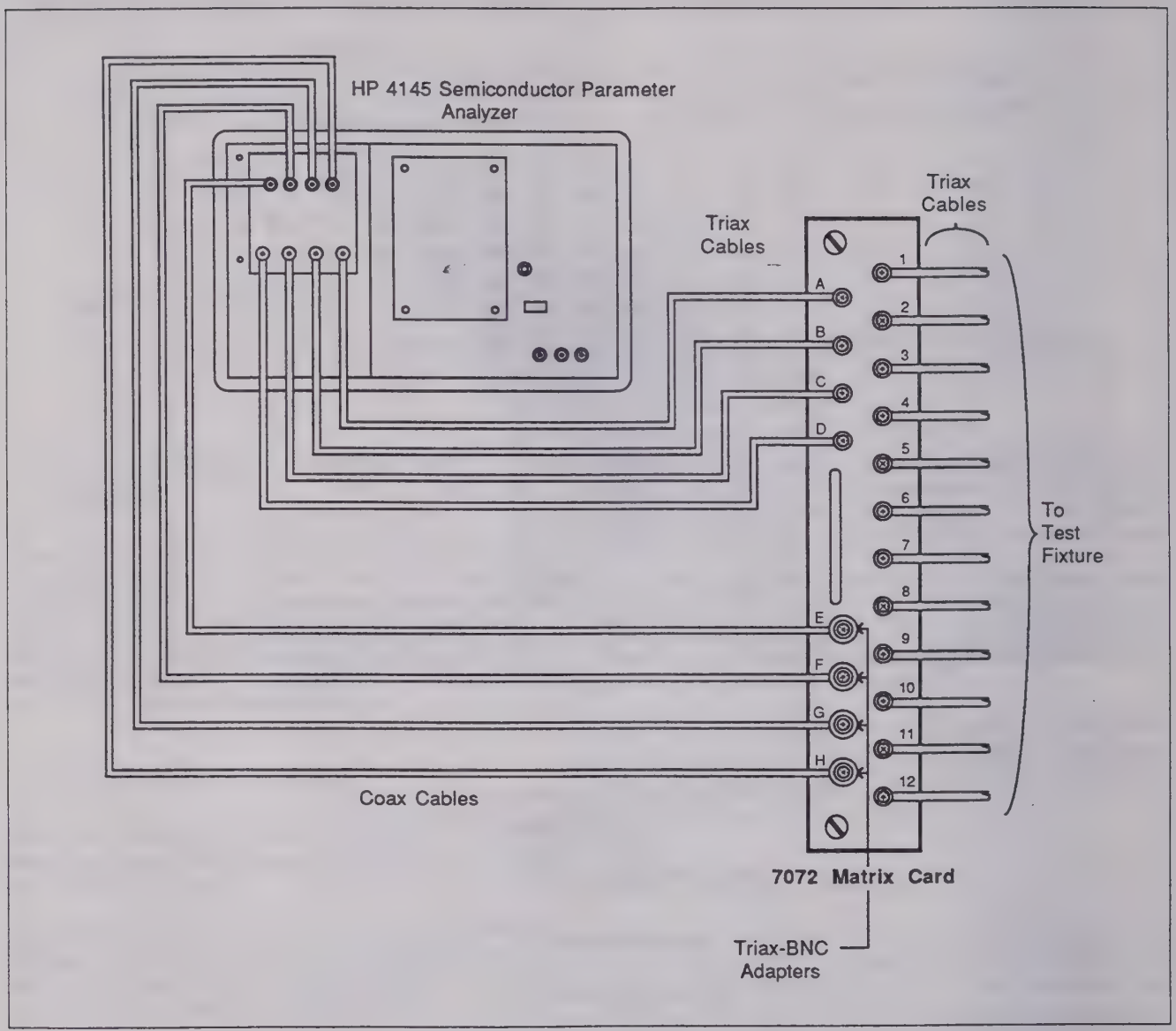


Figure 3-11. SPA Connections

Connections to a user-supplied test fixture should be made using triax cables in order to maintain path integrity and safety. BNC cables and adapters should not be used in case hazardous potential appears on guard terminals.

3.5.3 SPA Measurement Considerations

A complete discussion of SPA measurements is well beyond the scope of this manual. However, there are a few points that should be kept in mind when using this arrangement. Additional measurement considerations may be found in Section 2, paragraph 2.7 of this instruction manual.

Any switching system can degrade low-level signals, and the same hold true for the system shown in Figure 3-10. Since rows A and B on the Model 7072 are dedicated low current pathways, the SMUs that will source or sense low-level signals should be connected only to these rows. The remaining rows can be used for less-critical signals.

Safety considerations are also a concern when connecting instruments to a switching matrix. Therefore, it is strongly recommended that you carefully read the HP 4145B manual before using the system.

WARNING

Hazardous voltage may be present on the outer conductors of the connecting cables when the HP 4145B is set up for floating measurements.

3.5.4 Typical Test Procedure

The following paragraphs outline the procedure for using the SPA/matrix system to perform a typical test: V_{DS}–I_D (common-source) curves of a typical JFET. The procedure uses one of the four standard setups that are part of the applications package supplied with the HP 4145B.

System Configuration

Figure 3-12 shows the configuration and connections for this example. Only three of the four SMUs are required for the test, as indicated in the figure. A total of four FETs can be connected to a single card, as shown on the diagram. In all cases, triax cabling should be used. The crosspoints to close to test a specific FET are summarized in Table 3-3.

Table 3-3. Crosspoint Summary for JFET Test

JFET Tested	Crosspoints Closed* (Source, Gate, Drain)
1	A2, C1, B3
2	A5, C4, B6
3	A8, C7, B9
4	A11, C10, B12

* Crosspoints from Figure 3-12.

Procedure

1. Connect the system and devices together, as shown in Figure 3-12.
2. Turn on the HP 4145B and allow it to go through its boot-up routine.
3. Turn on the Model 707 Switching Matrix.
4. From the HP 4145B main menu, select the channel definition page, then choose the FET V_{DS}–I_D application.
5. Press the PAGE NEXT key, and program the source parameters, as required.
6. Press the PAGE NEXT key, and program the required graphing parameters.
7. Press the PAGE NEXT key to display the graph format.
8. From the front panel of the Model 707, close the crosspoints necessary to connect the FET being tested to the SMUs (see Table 3-3).
9. Press the MEASUREMENT SINGLE key to initiate the sweep. The SPA will generate the I_D vs. V_{DS} curves at specified V_{GS} values.
10. Open the crosspoints presently closed.
11. Repeat steps 8 and 9 for the remaining devices, as required.

Typical Plot

Figure 3-13 shows a typical plot made using the procedure above. The device tested was a 2N4392 N-channel JFET. For the graphs, V_{DS} was swept from 0V to 10V in 0.1V increments, and V_{GS} was stepped from 0 to −0.25V.

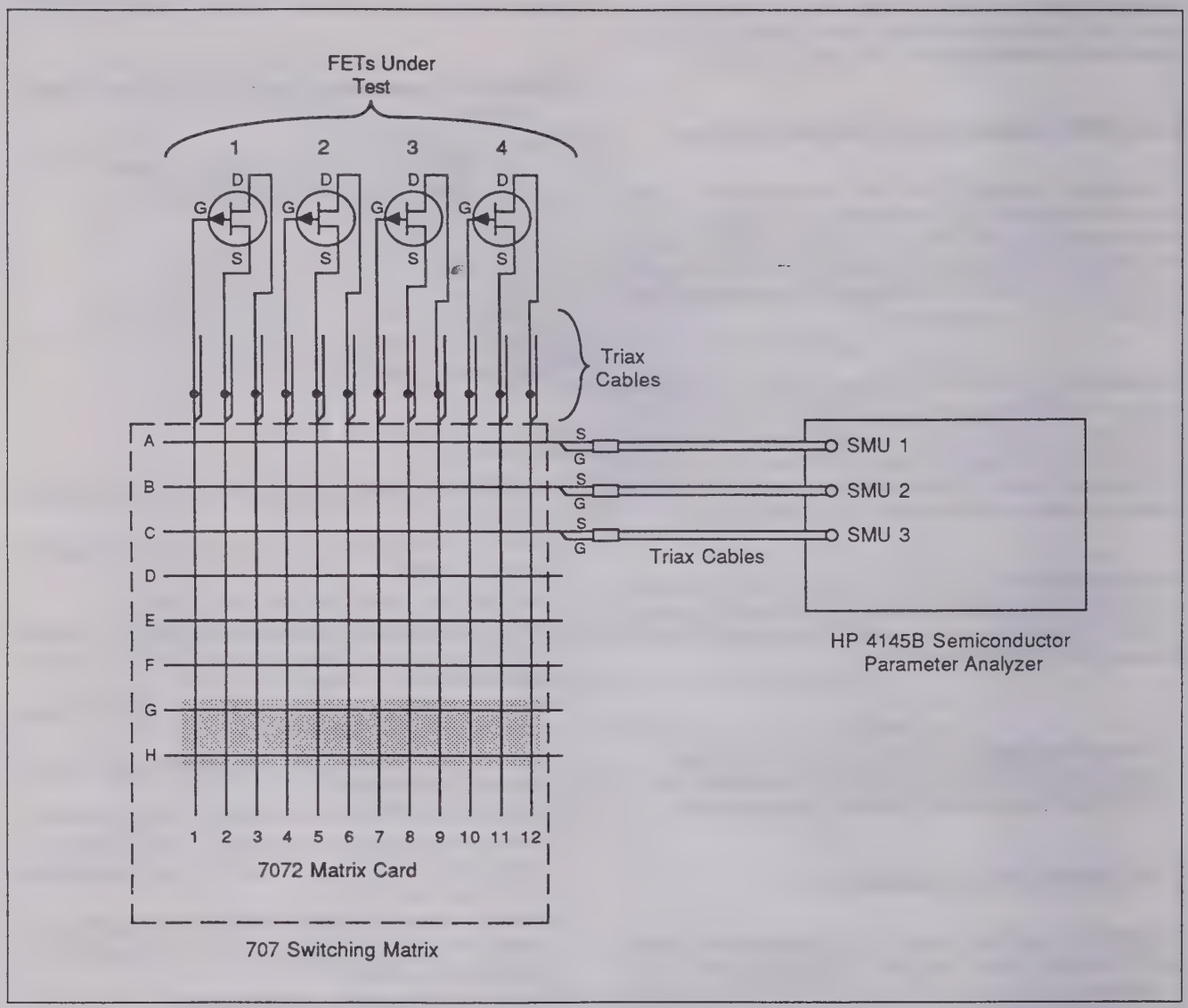


Figure 3-12. System Configuration for JFET Test

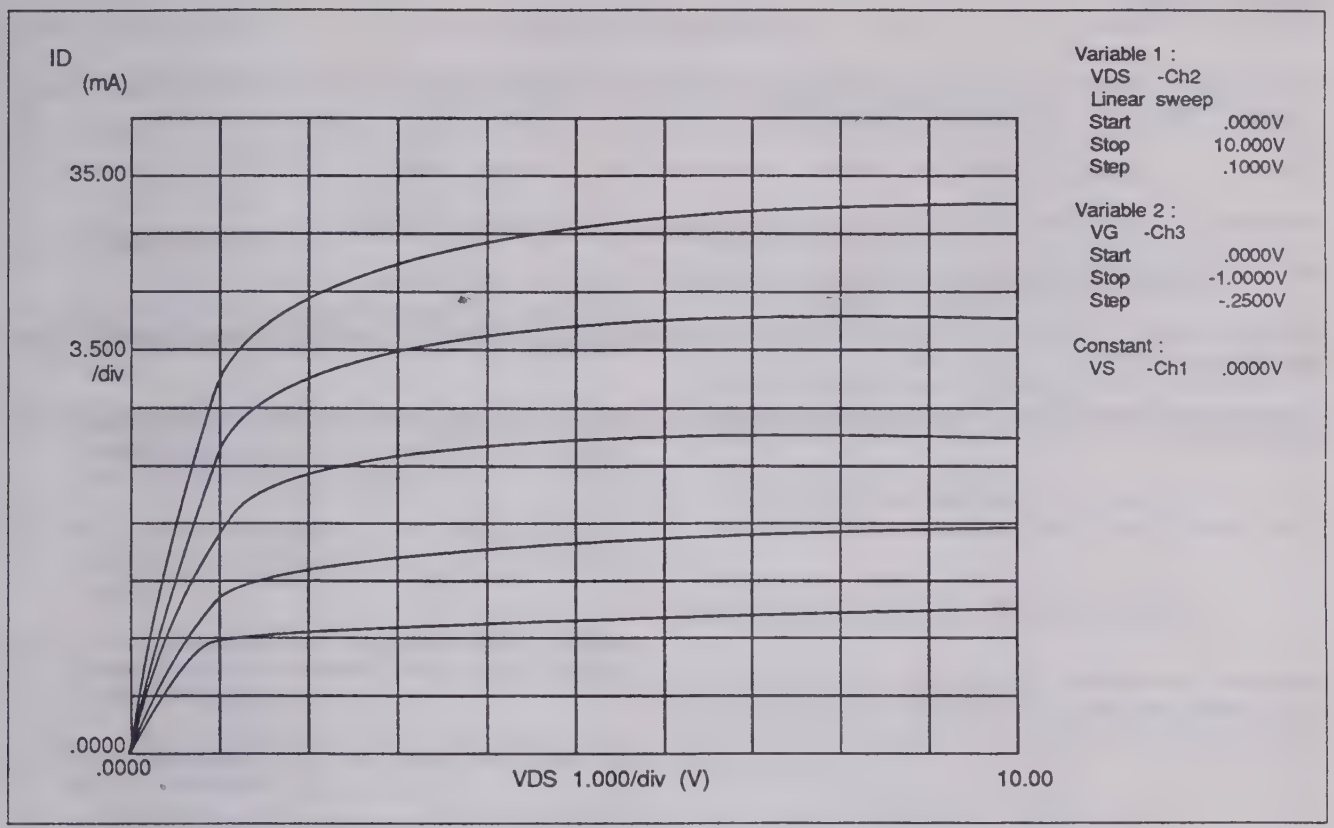


Figure 3-13. Typical JFET Plot

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SECTION 4
Service Information

4.1 INTRODUCTION

This section contains information necessary to service the Model 7072 Semiconductor Matrix Card and is arranged as follows:

4.2 **Handling and Cleaning Precautions:** Discusses handling precautions and methods to clean the card should it become contaminated.

4.3 **Performance Verification:** Covers the procedures necessary to determine if the card is operating properly.

4.4 **Special Handling of Static-Sensitive Devices:** Reviews precautions necessary when handling static-sensitive devices.

4.5 **Troubleshooting:** Presents some troubleshooting tips for the Model 7072.

4.6 **Principles of Operation:** Briefly discusses circuit operation.

4.2 HANDLING AND CLEANING PRECAUTIONS

Because of the high-impedance circuits on the Model 7072, care should be taken when handling or servicing the card to prevent possible contamination. The following precautions should be taken when servicing the card.

1. Handle the card only by the edges and handle (do not touch the edge connectors). Do not touch any board surfaces or components not associated with the repair.
2. Do not store or operate the card in an environment where dust could settle on the circuit board. Use dry nitrogen gas to clean dust off the board if necessary.
3. Should it become necessary to use solder on the circuit board, remove the flux from the work areas when the repair has been completed. Use Freon® TMS or TE or the equivalent along with clean cotton swabs or a clean, soft brush to remove the flux. Take care not to spread the flux to other areas of the circuit board. Once the flux has been removed, swab only the repaired area with methanol, then blow dry the board with dry nitrogen gas.
4. After cleaning, the card should be placed in a 50°C low-humidity environment for several hours before use.

4.3 PERFORMANCE VERIFICATION

The following paragraphs discuss performance verification procedures for the Model 7072, including relay testing, contact resistance, contact potential, path isolation, and leakage current.

4.3.1 Environmental Conditions

All verification measurements except for path isolation and offset current should be made at an ambient temperature between 0°C and 35°C and at a relative humidity of less than 70%. Path isolation and offset current verification must be performed at an ambient temperature of 23°C and at a relative humidity of less than 60% If the matrix card has be subjected to temperature or humidity extremes, allow the card to environmentally stabilize for at least one hour before performing any tests.

4.3.2 Recommended Test Equipment

Table 4-1 summarizes the equipment necessary to make the performance verification tests, along with the application for each item.

Table 4-1. Recommended Verification Equipment

Qty	Description	Application
1	Model 617 Electrometer	Offset current; path isolation
1	Model 196 6½ Digit DMM	Path resistance
1	Model 707 Switching Matrix	All tests
1	IBM PC or HP 200 or 300 computer	Relay test
4	Model 7078-TRX-10 triax cables*	Offset current; path resistance
2	Model 7078-TRX-3 triax cables	Path isolation, offset current
1	Model 6172 2-slot male to 3-lug female triaxial adapter	Offset current
3	Model 7078-TRX-T triax tee adapter	Path resistance
5	Banana plugs (part #B6-10-2)*	Path isolation and resistance
1	Relay test terminal block*	Relay test

*These items are used to construct special cables; see text.

4.3.3 Relay Testing

The relays on Model 7072 can be tested using the test software supplied with the Model 707 Switching Matrix. The following paragraphs discuss the test equipment and connections. For detailed information on using the test software, consult Section 6 of the Model 707 Instruction Manual.

Recommended Equipment

- Model 707 Switching Matrix
- Unterminated 3-slot triax cables (2), made by cutting one TRX-7078-10 cable in half
- Relay test software (supplied with Model 707)
- IBM PC compatible or Hewlett Packard Series 200 or 300 computer
- Relay test connector (supplied with Model 707)

Connections

The test cable should be prepared using the information shown in Figure 4-1. The center conductor of the unterminated end of one triax cable should be connected to pin 1 of the relay test connector, while the inner shield should be connected to pin 2. The outer shield should be cut off and be left floating at the test connector end.

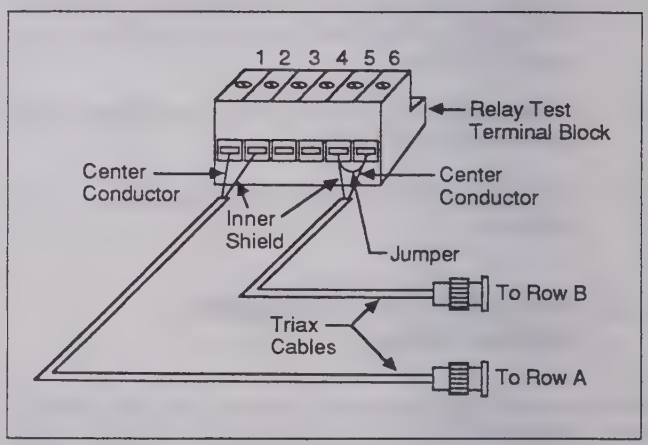


Figure 4-1. Test Cable Preparation

The remaining triax cable should be connected as follows: connect the center conductor to pin 6, and connect the inner shield to pin 5. Again, the outer shield should be left floating. Also, jumper pins 5 and 6 of the relay test connector together.

Figure 4-2 shows how to connect the prepared test cable to the Model 7072. Connect the first triax cable to row A of the card, and connect the second triax cable to row B. Also be sure to connect the test connector to the RELAY TEST jack on the rear panel of the Model 707.

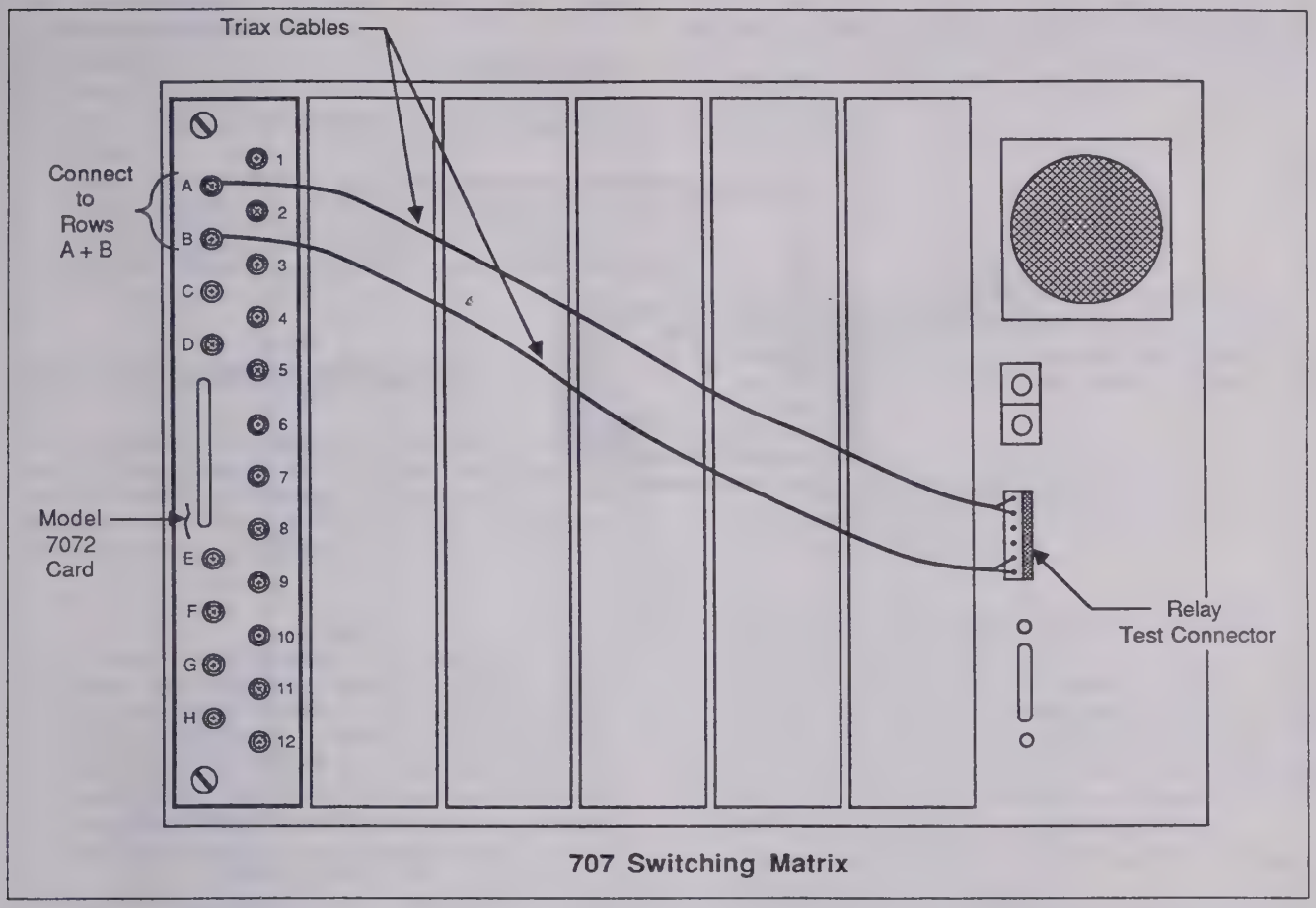


Figure 4-2. Connecting the Test Cable to the Model 7072

Running the Test

Follow the instructions given in the Model 707 Instruction Manual to perform the relay test. The computer will advise you as to which relay or group of relays (if any) fail to pass the test.

4.3.4 Offset Current Verification

Recommended Equipment

- Model 707 Switching Matrix
- Model 617 Electrometer
- Model 7078-TRX-3 Triax Cable
- Model 6172 2-slot male to 3-lug female triaxial adapter

Test Connections

Figure 4-3 shows the test connections for offset current verification. The Model 7072 row being tested is to be connected to the Model 617 Electrometer input through the triaxial cable and the triaxial adapter. Note that the electrometer ground strap is to be removed, and the electrometer should be operated in the unguarded mode.

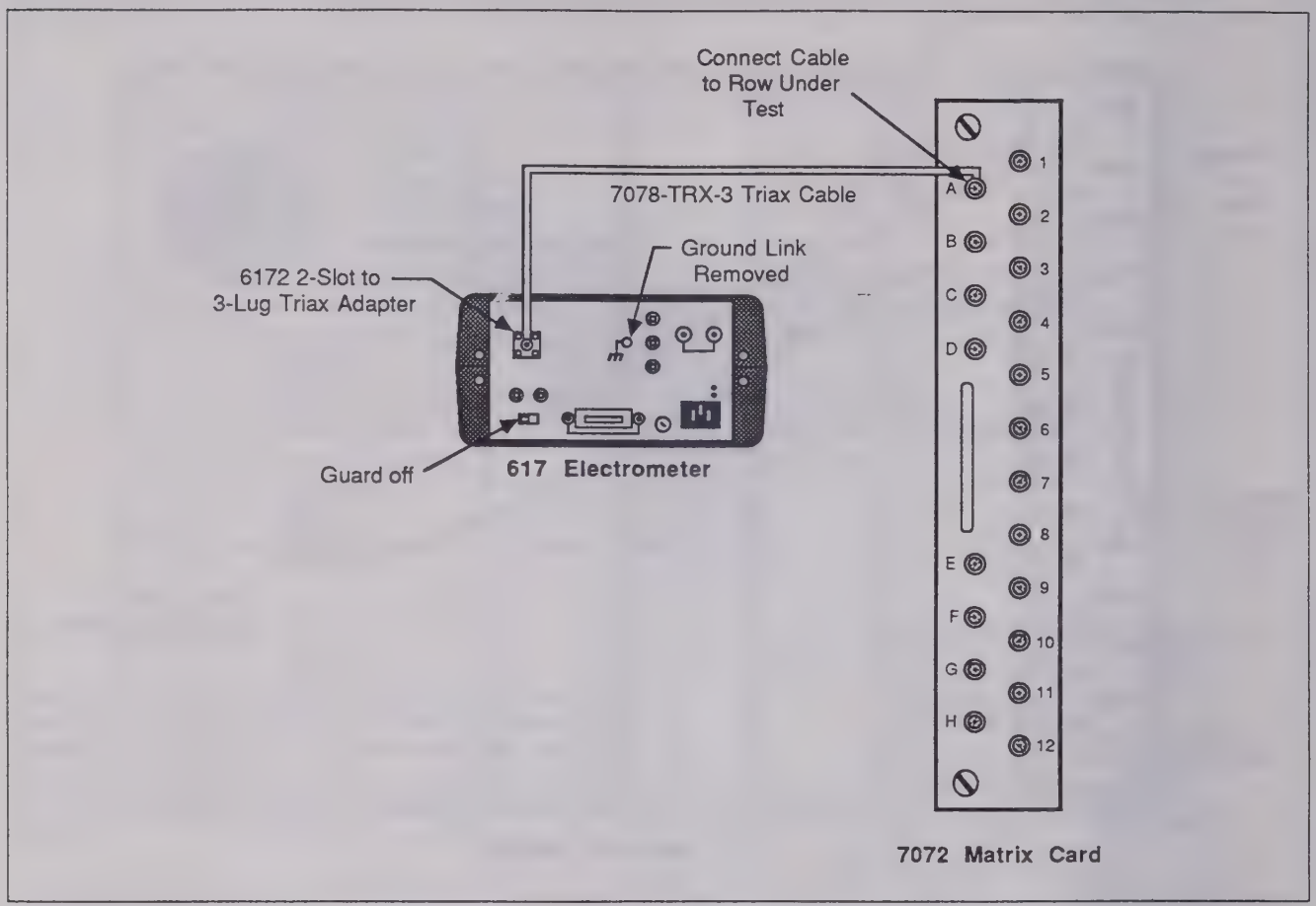


Figure 4-3. Offset Verification Test Connections

Procedure

NOTE

The following procedure should be performed at an ambient temperature of 23°C and at a relative humidity of less than 60%.

1. Turn on the Model 617 power and allow it to warm up for two hours before beginning the verification procedure.
2. With the power off, install the Model 7072 in the desired slot of the Model 707 Switching Matrix. Remove all other cards from the instrument, and install the slot covers.
3. After the prescribed warm up period, select the amps function and the 2pA range on the Model 617. Zero correct the instrument, and then select autoranging.
4. Connect the Model 617 to row A of the Model 7072, as shown in Figure 4-3.
5. Close crosspoint A1 by using the Model 707 front panel controls.
6. Disable zero check on the Model 617, and allow the reading to settle.
7. Verify that the offset current reading is <1pA.
8. Enable zero check on the Model 617, and open crosspoint A1.
9. Repeat steps 5 through 8 for crosspoints A2 through A12. Only one crosspoint at a time should be closed.
10. Disconnect the triax cable from row A, and connect it instead to row B.
11. Repeat steps 5 through 8 for crosspoints B1 through B12. Only one crosspoint at a time should be closed.
12. With zero check enabled, disconnect the electrometer from row B, and connect it to row C.

13. Close crosspoint C1 by using the front panel controls of the Model 707.
14. Disable zero check, and allow the reading to settle.
15. Verify that the offset current reading is <20pA.
16. Enable zero check, then open the crosspoint presently closed.
17. Repeat steps 12 through 16 for rows D through H. The electrometer should be connected to the row being tested, and only one crosspoint must be closed at a time. The offset current for each crosspoint should be <20pA.

4.3.5 Path Isolation Verification

The procedure for verifying path isolation is discussed below. Should the card fail any of the tests, clean it using the procedures outlined in paragraph 4.2. If rows C through F still fail, the problem may lie in contamination of the mainframe backplane.

NOTE

If the path isolation for specific rows is below standards, test the associated rows or columns with the card removed from the mainframe. (Of course, it will not be possible to close crosspoints with the card removed.) If rows C-F pass with the card removed but fail with the card installed, the backplane in the mainframe may require cleaning. See the Model 707 Instruction Manual.

Recommended Equipment

- Model 707 Switching Matrix
- Model 617 Electrometer
- Model 7078-TRX-3 triaxial cable
- Unterminated 3-slot triaxial cable (cut connector off 7078-TRX-3)
- Banana plug (Keithley part #BG-10-2)
- #16-18AWG insulated stranded wire (6 in. length)

Test Connections

Figure 4-4 shows the test connections for the path isolation tests. One row being tested is to be connected to the Model 617 Electrometer input through a Model 6172 2-slot female to 3-lug male triaxial adapter. The other row is to be connected to the voltage source HI terminal using a specially prepared 3-slot triax-to-banana plug cable, the construction of which is shown in Figure 4-5. Note that both the inner shield and the center conductor are to be connected to the banana plug as shown.

COM and the LO terminal of the electrometer voltage source must be connected together as shown. Also, the ground link between COM and chassis must be removed, and the Model 617 guard must be turned off for current measurements.

Procedure

WARNING

Hazardous voltage from the electrometer voltage source will be used in the following steps. Take care not to contact live circuits, which could cause personal injury or death.

NOTE

The following procedure must be performed at an ambient temperature of 23°C and at a relative humidity of less than 60%.

1. Turn on the Model 617 and allow it to warm up for two hours for rated accuracy.
2. With the mainframe power turned off, plug the Model 7072 into slot 1 of the mainframe. Remove all other cards from the mainframe, and install the slot covers.
3. After the prescribed warm up period, select the Model 617 amps function, and enable zero check. Select the 2pA range, and zero correct the instrument.
4. Connect the Model 617 to rows A and B of the matrix card, as shown in Figure 4-4.
5. Program the Model 617 voltage source for a value of +100V, but do not yet turn on the voltage source output.
6. Close crosspoints A1 and B2 by using the switching matrix front panel controls.
7. With the Model 617 in amps, enable suppress after the reading has settled.
8. Turn on the Model 617 voltage source output, and enable the V/I ohms function on the electrometer.
9. After the reading has settled, verify that the resistance is >10TΩ ($10^{13}\Omega$).
10. Turn off the voltage source, and enable zero check. Disable suppress, and select the amps function on the electrometer.
11. Open crosspoints A1 and B2, and close crosspoints A3 and B4.
12. Repeat steps 7 through 11 for A3 and B4.
13. Repeat steps 7 through 12 for crosspoint pairs A5 and B6, A7 and B8, A9 and B10, and A11 and B12.
14. Disconnect the electrometer from rows A and B, and connect it instead to rows C and D.

15. Repeat steps 7 through 13 for rows C and D. The path isolation for these rows should be >1TΩ ($10^{12}\Omega$).
16. Repeat steps 7 through 14 for row pairs E and F, and G and H. For each row pair, step through the crosspoint pairs 1 and 2, 3 and 4, 5 and 6, 7 and 8, 9 and 10, and 11 and 12. The complete procedure outlined in steps 7 through 11 should be repeated for each crosspoint pair. Each resistance measurement for rows E through H should be >1TΩ ($10^{12}\Omega$).

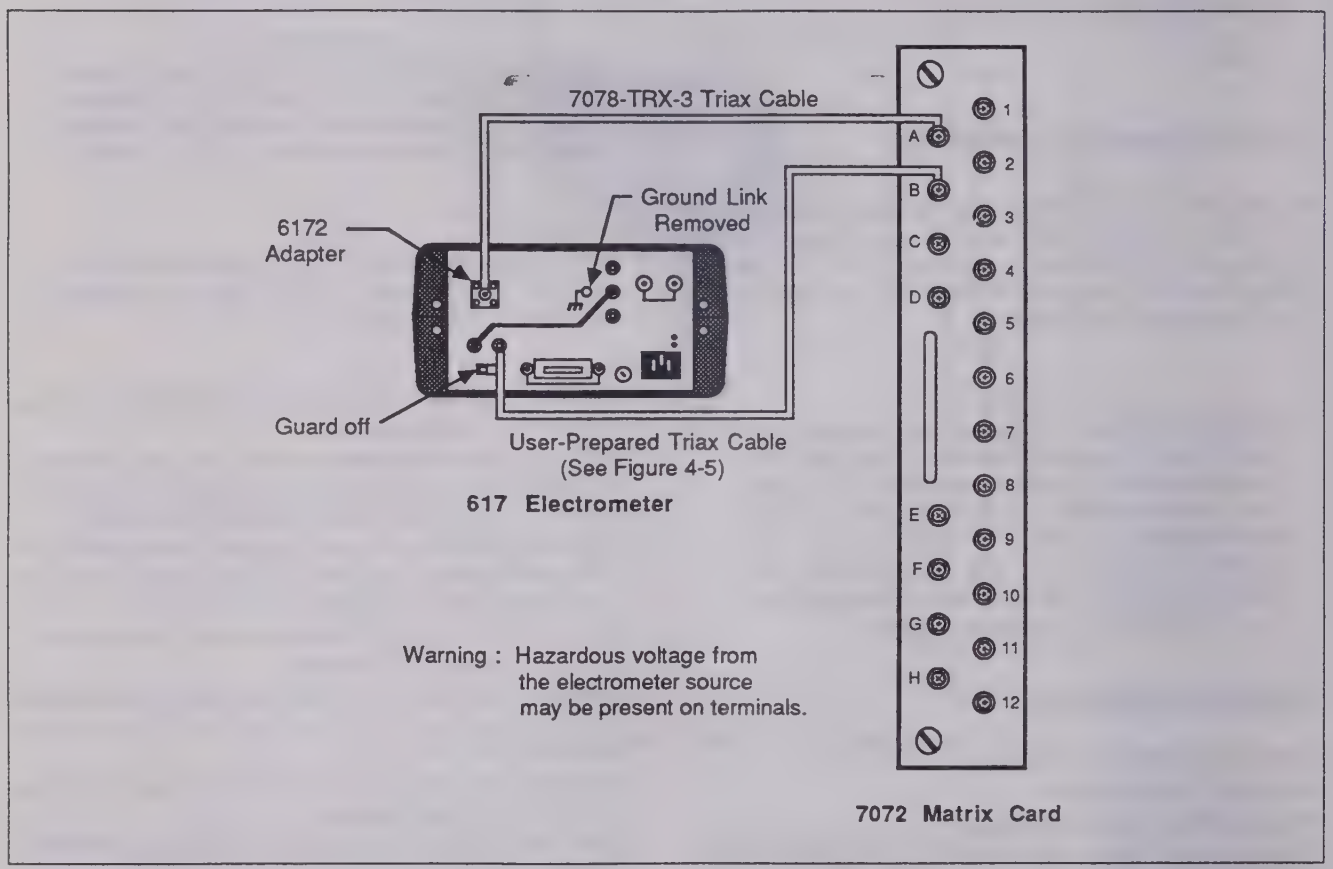
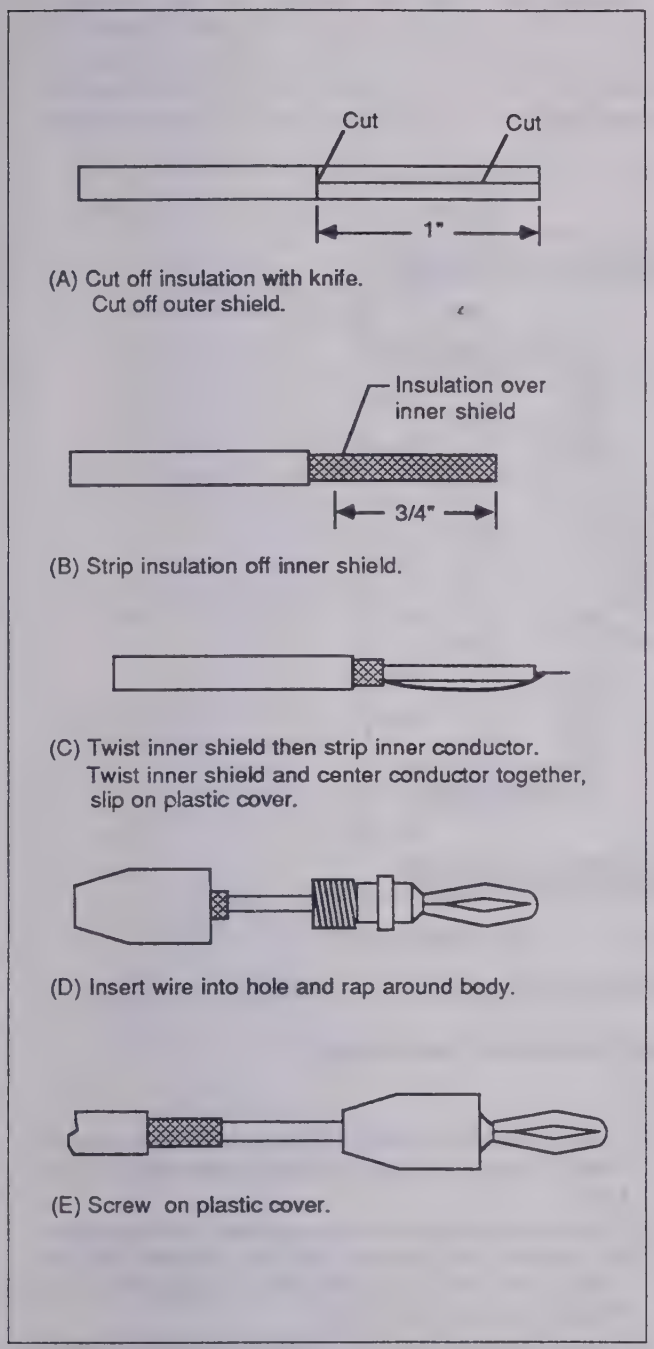


Figure 4-4. Connections for Path Isolation Verification



(A) Cut off insulation with knife. Cut off outer shield.

(B) Strip insulation off inner shield.

(C) Twist inner shield then strip inner conductor. Twist inner shield and center conductor together, slip on plastic cover.

(D) Insert wire into hole and rap around body.

(E) Screw on plastic cover.

Figure 4-5. Triaxial Cable Preparation

4.3.6 Path Resistance Verification

The following paragraphs discuss the equipment, connections, and procedure to check path resistance. Should a particular pathway fail the resistance test, the relay (or relays) for that particular crosspoint is probably defective. See the schematic diagram at the end of Section 5 to determine which relay is defective.

Recommended Equipment

- Model 196 DMM
- 7078-TRX-T triax tee adapters (3)
- Unterminated 3-slot triax cables (4), made from two 7078-TRX-10 triax cables.
- Banana plugs (4), Keithley part number BG-10-2

Connections

Figure 4-6 shows the connections for the path resistance tests. The Model 196 is to be connected to the row and column jacks using prepared triax/banana cables (Figure 4-5, but with inner shield and center conductor disconnected.) and 7078-TRX-T triax tee adapters. The special cables can be made from two 7078-TRX-10 cables each cut in half, or four 7078-TRX-3 cables by cutting one triax connector off each cable.

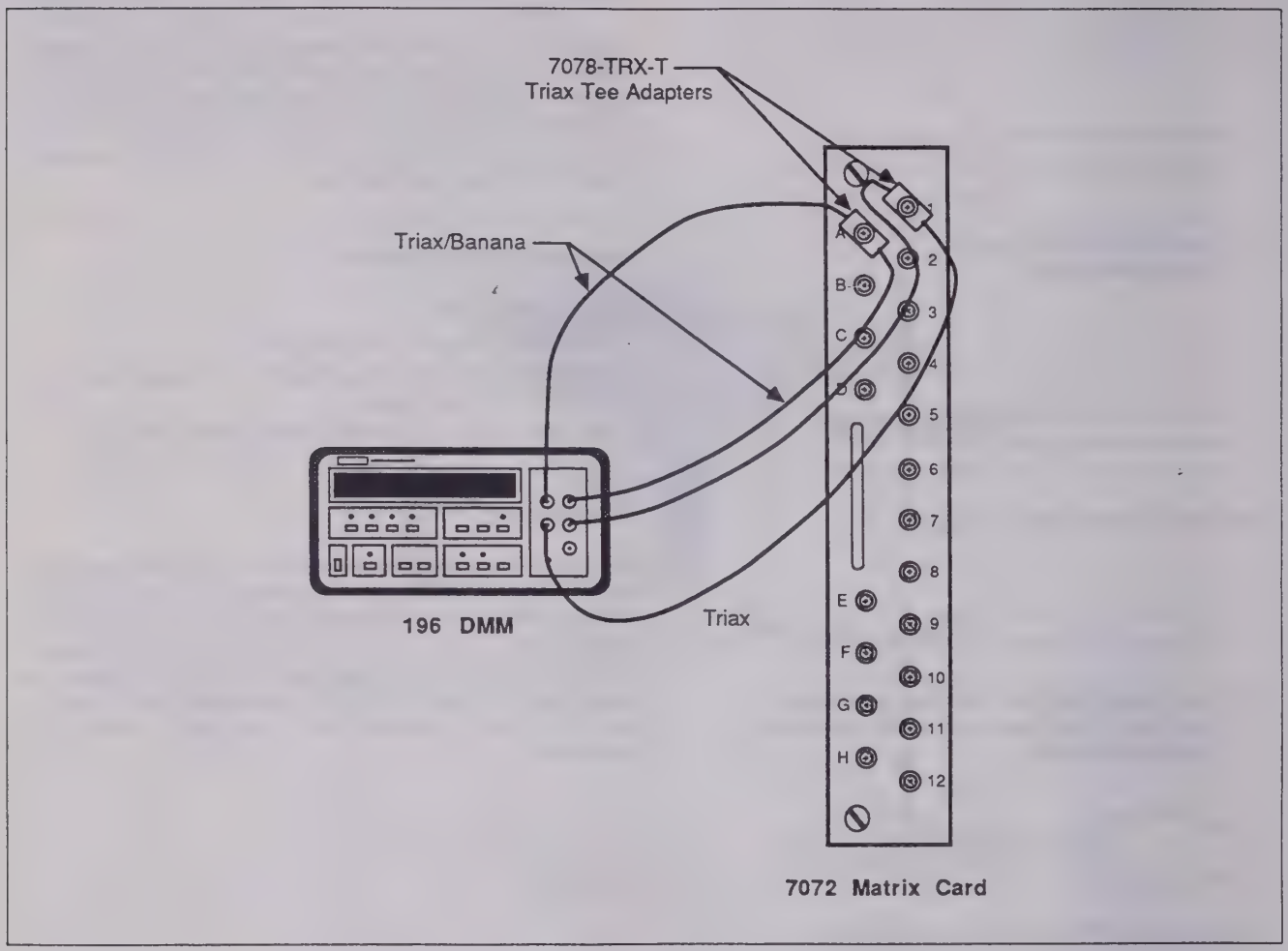


Figure 4-6. Connections for Path Resistance Verification

Procedure

1. Turn on the Model 196 DMM and allow it to warm up for at least one hour before beginning the test.
2. With the power off, install the Model 7072 card in slot 1 of the mainframe.
3. Connect the four triaxial cables to the Model 196 and the two triax tee adapters (Figure 4-6), but do not yet connect the adapters to the Model 7072.
4. Temporarily connect the two triax tee connectors together using a third triax tee adapter, as shown in Figure 4-7.
5. Select the ohms function, 300Ω range, and 6½-digit resolution on the Model 196.
6. After the reading settles, enable zero on the Model 196 DMM. Leave zero enabled for the remainder of the tests.
7. Disconnect the two triax tee adapters from the shorting adapter, and connect the two adapters with the cable to the row A and column 1 connectors on the Model 7072 (see Figure 4-6).
8. Close crosspoint A1, and allow the reading to settle.
9. Verify that the resistance reading is $<3.5\Omega$.
10. Open the crosspoint, and disconnect the triax adapter from column 1. Connect the adapter to column 2.
11. Repeat steps 8 through 10 for columns 2 through 12. In each case, the column adapter must be connected to the column under test, and the crosspoint must be closed.

12. Disconnect the row adapter from row A, and connect it instead to row B.
13. Repeat steps 8 through 10 for row B. The crosspoints of interest here are B1 through B12. Also, the row adapter must be connected to the row being tested.
14. Repeat steps 8 through 13 for rows C through H. In each case, the crosspoint to close is the one corresponding to the row and column connections at that time. In all cases, the measured resistance should be $<3.5\Omega$.

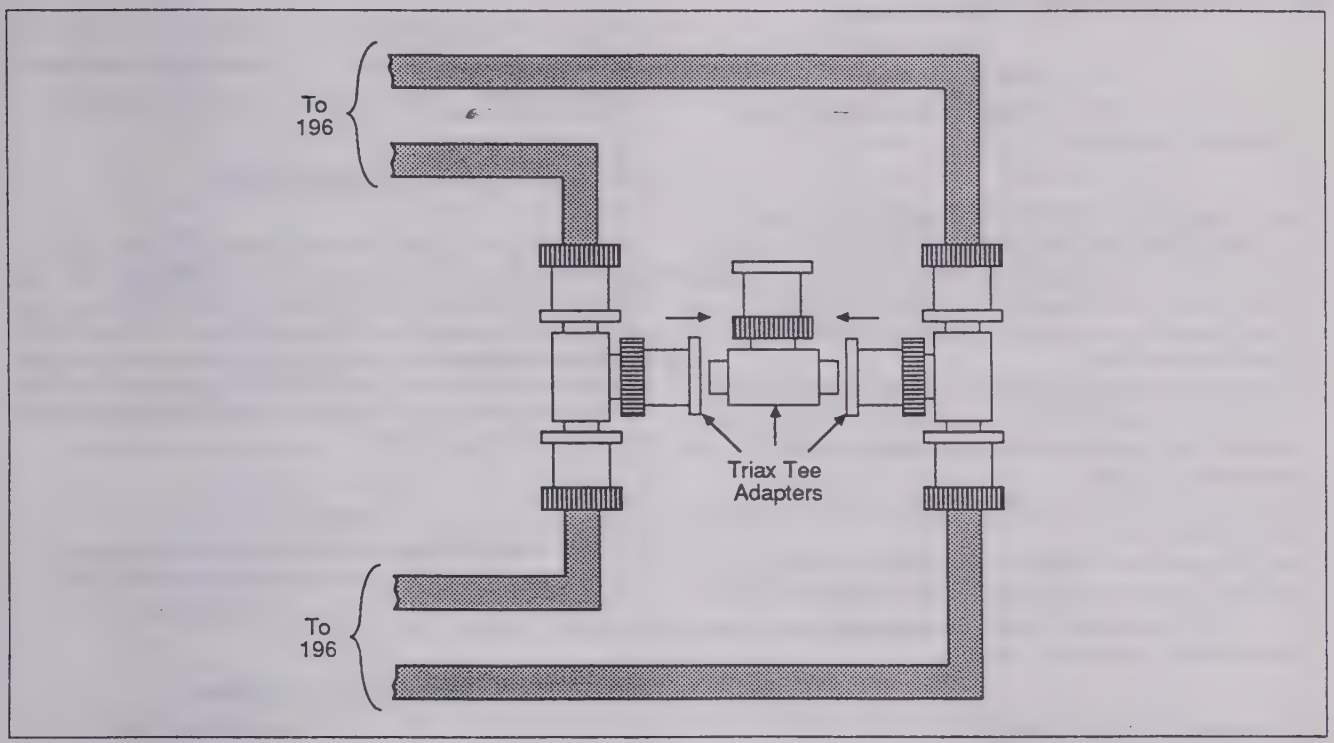


Figure 4-7. Shorting Measurement Paths Using Triax Tee Adapter

4.4 SPECIAL HANDLING OF STATIC-SENSITIVE DEVICES

CMOS and other high-impedance devices are subject to possible static discharge damage because of the high-impedance levels involved. When handling such devices, use the precautions listed below.

NOTE
In order to prevent damage, assume that all parts are static sensitive.

1. Such devices should be transported and handled only in containers specially designed to prevent or dissipate static build-up. Typically, these devices will be received in anti-static containers made of plastic or foam. Keep these parts in their original containers until ready for installation or use.
2. Remove the devices from their protective containers only at a properly-grounded work station. Also ground yourself with an appropriate wrist strap while working with these devices.
3. Handle the devices only by the body; do not touch the pins or terminals.
4. Any printed circuit board into which the device is to be inserted must first be grounded to the bench or table.
5. Use only anti-static type de-soldering tools and grounded-tip soldering irons.

4.5 TROUBLESHOOTING

4.5.1 Recommended Equipment

Table 4-2 summarizes the recommended equipment for general troubleshooting.

Table 4-2. Recommended Troubleshooting Equipment

Description	Manufacturer and Model	Application
5½-Digit DMM	Keithley 199	Measure DC voltages
Oscilloscope	TEK 2243	View logic waveforms
Extender card	Keithley 7070	Allow circuit access

4.5.2 Using the Extender Card

In order to gain access to the test points and other circuitry on the Model 7072, the card must be plugged into the Model 7070 Extender Card, which, in turn, must be plugged into the desired slot of the mainframe. The Model 7070 must be configured as an extender card by placing the configuration jumper in the EXTEND position. See the documentation supplied with the Model 7070 for complete details on using the card.

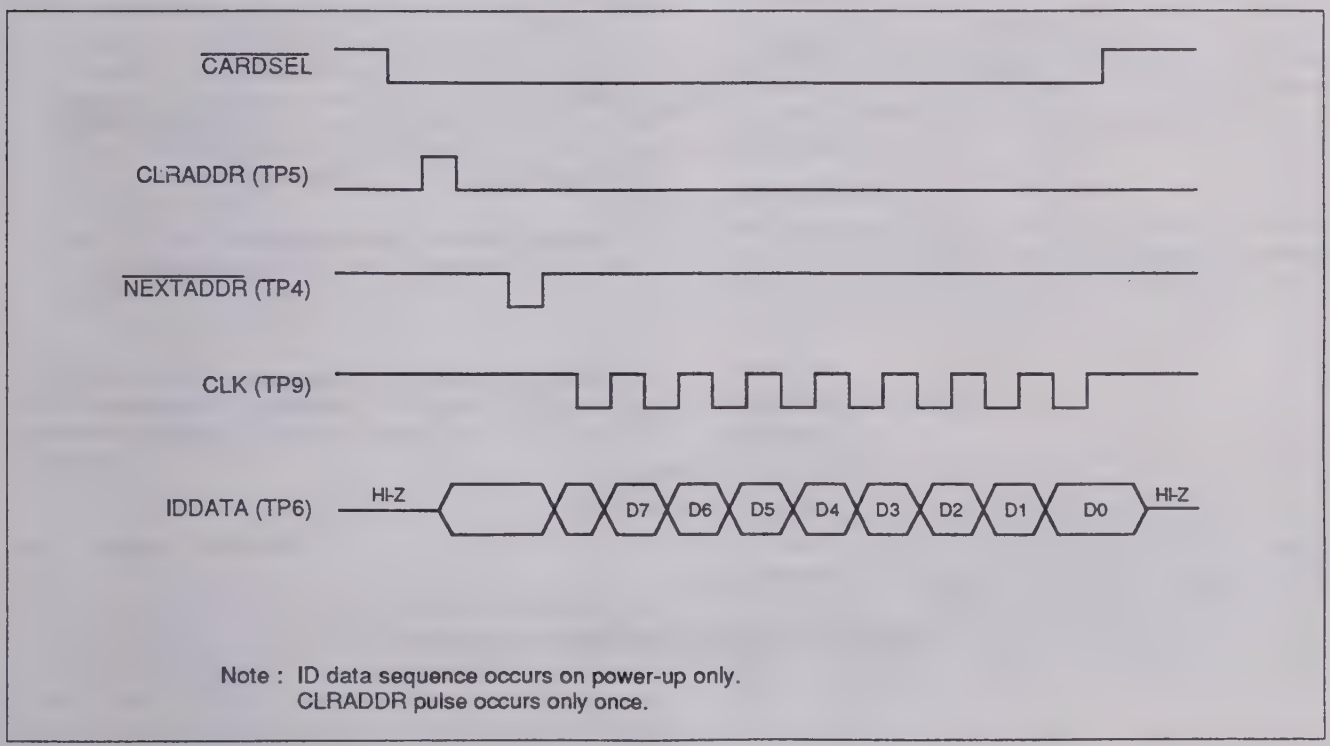
NOTE
The Model 7070 cannot be used for performing the verification tests because its presence will affect the results.

4.5.3 Troubleshooting Procedure

Table 4-3 summarizes the troubleshooting procedure for the Model 7072 Semiconductor Matrix Card. Some of the troubleshooting steps refer to the ID data timing diagram shown in Figure 4-8. In addition to the procedure shown, the relay tests outlined in paragraph 4.3.3 can be used to aid in troubleshooting. Also, refer to paragraph 4.6 for an overview of operating principles.

Table 4-3. Troubleshooting Procedure

Step	Item/Component	Required Condition	Comments
1	TP2		All voltages referenced to TP2 (digital common)
2	TP1	+6VDC	Relay voltage
3	TP3	+5VDC	Logic voltage
4	TP4	NEXT ADDR pulses	Power up only (Fig. 4-8)
5	TP5	CLR ADDR pulse	Power up only (Fig. 4-8)
6	TP6	ID data pulses	Power up only (Fig. 4-8)
7	TP7	STROBE pulse	End of relay data sequence.
8	TP8	Relay data (128 bits)	Present when updating relays.
9	TP9	CLK pulses	Present during relay data or ID data.
10	TP10	High on power up until first STROBE sets low.	Power on safe guard.
11	U30-U45, pins 10-18	Low with relay energized, high with relay de-energized.	Relay driver outputs



Note : ID data sequence occurs on power-up only.
CLRADDR pulse occurs only once.

Figure 4-8. ID Data Timing

4.6 PRINCIPLES OF OPERATION

The following paragraphs discuss the basic operating principles for the Model 7072. A schematic diagram of the matrix card may be found in drawing number 7072-106 (four sheets), located at the end of Section 5.

4.6.1 Block Diagram

Figure 4-9 shows a simplified block diagram of the Model 7072. Key elements include the buffer (U46), ID data circuits (U14, U27, and U47), relay drivers (U30-U45) and relays (K1-K128), and power-on safe guard (U29). The major elements are discussed below.

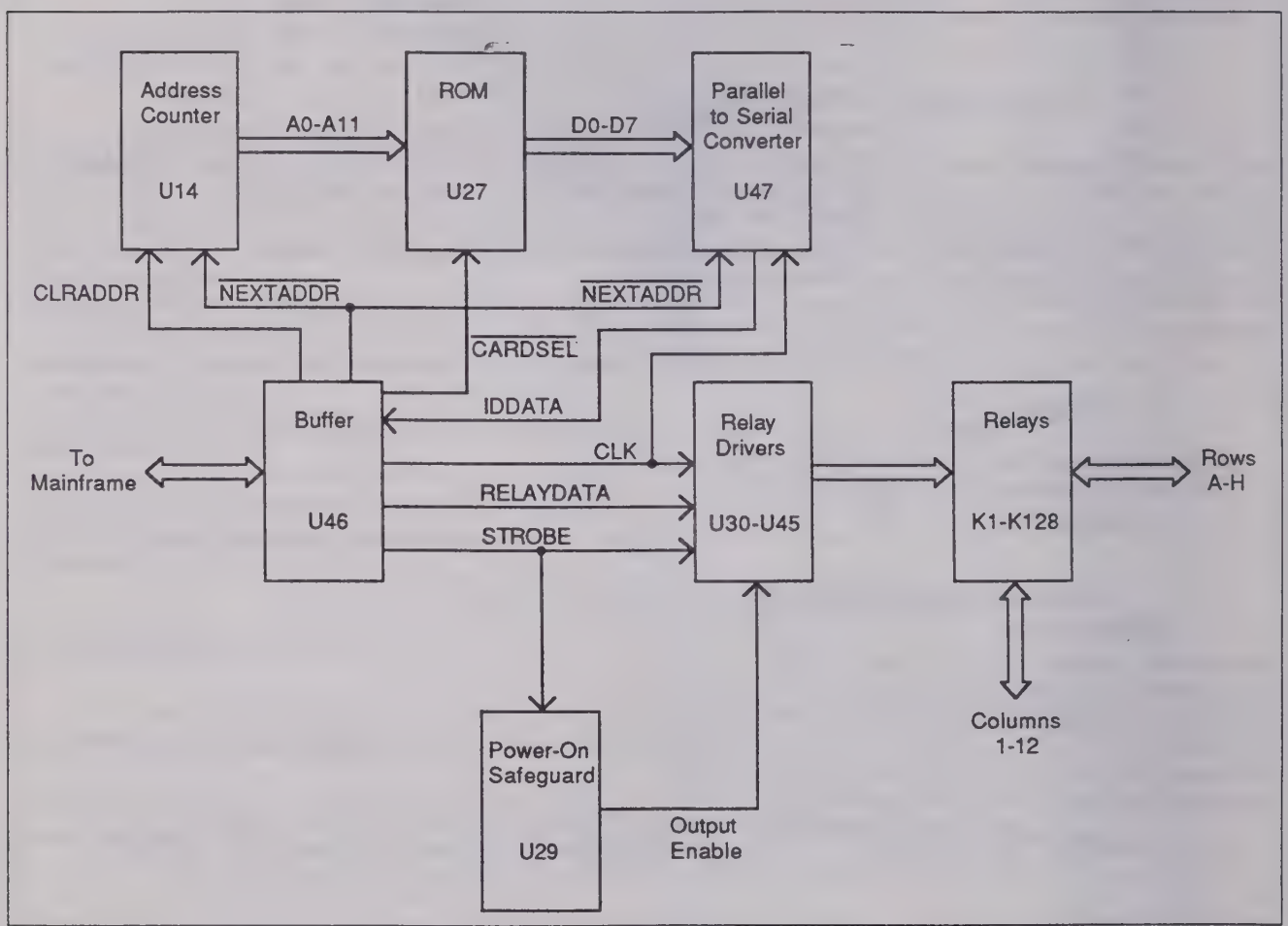


Figure 4-9. Model 7072 Block Diagram

4.6.2 ID Data Circuits

Upon power up, the card identification data information from each card is read by the mainframe. This ID data includes such information as card ID, hardware settling time for the card, and a relay configuration table, which tells the mainframe which relays to close for a specific crosspoint. This configuration table is necessary because some cards (such as the Model 7072) require the closing of more than one relay to close a specific crosspoint.

ID data is contained within an on-card ROM, U27. In order to read this information, the sequence below is performed upon power up. Figure 4-8 shows the general timing of this sequence.

1. The CARDSEL line is brought low, enabling the ROM outputs. This line remains low throughout the ID data transmission sequence.
2. The CLRADDR line is pulsed high to clear the address counter and set it to zero. At this point, a ROM address of zero is selected. This pulse occurs only once.
3. The NEXTADDR line is set low. NEXTADDR going low increments the counter and enables parallel loading of the parallel-to-serial converter. NEXTADDR is kept low long enough for the counter to increment and the ROM outputs to stabilize. This sequence functions because the load input of the parallel-to-serial converter is level sensitive rather than edge sensitive. The first ROM address is location 1, not 0.
4. The CLK line clocks the parallel-to-serial converter to shift all eight data bits from the converter to the mainframe via the IDDATA line.

The process in steps 3 and 4 repeats until all the necessary ROM locations have been read. A total of 498 bytes of information are read by the mainframe during the card ID sequence.

4.6.3 Relay Control

The relays are controlled by serial data transmitted via the RELAYDATA line. A total of 16 bytes for each card are shifted in in serial fashion into latches located in the 16 relay drivers, U30-U45. The serial data is fed in through the DATA lines under control of the CLK signal. As data overflows one register, it is fed out the Q'S line of that register to the next IC down the chain.

Once all 16 bytes have been shifted into each card in the mainframe, the STROBE line is set high to latch the relay information into the Q outputs of the relay drivers, and the appropriate relays are energized (assuming the driver outputs are enabled, as discussed below). Logic convention is such that the corresponding relay driver output must be low to energize the associated relay, while the output is high when the relay is de-energized. For example, if the Q1 output of U35 is low, relay K1 will be energized.

4.6.4 Power-on Safeguard

A power-on safeguard circuit, made up of U29 and associate components, ensures that relays do not randomly energize upon power-up. The two AND gates, U29, make up an R-S flip-flop. Initially, the Q output of the flip-flop (pin 3 of U29) is set high upon power up. Since the OEN terminals of the relay drivers U30-U45 are held high, their outputs are disabled, and all relays remain de-energized regardless of the relay data information present at that time.

The first STROBE pulse that comes along (in order to load relay data) clears the R-S flip-flop, setting the OEN lines of U30-U45 low to enable their outputs. This action allows the relays to be controlled by the transmitted relay data information.

A hold-off period of approximately 470msec in included in the safeguard circuit to guard against premature enabling of the relays. The time constant of the hold-off period is determined by the relative values of R1 and C20.

4.6.5 Isolator Relays

Row and column isolator relays are necessary in addition to the crosspoint relays in order to ensure the integrity of low-level signal pathways (rows A, B, G, and H). Row isolator relays include K121 through K128, while column isolators are K25 through K36, and K85 through K96. The necessary isolator relay(s) are closed in addition to the selected crosspoint to complete the entire pathway. For example, if crosspoint C10 is closed, relays K34, K46, and K123 would be energized.

SECTION 5
Replaceable Parts

5.1 INTRODUCTION

This section contains a list of replaceable electrical and mechanical parts for the Model 7072, as well as a component layout drawing and schematic diagram of the matrix card.

5.2 PARTS LISTS

Electrical parts are listed in order of circuit designation in Table 5-1. Table 5-2 summarizes mechanical parts.

5.3 ORDERING INFORMATION

To place an order, or to obtain information about replacement parts, contact your Keithley representative or the factory (see the inside front cover of this manual for addresses). When ordering parts, be sure to include the following information:

1. Matrix card model number (7072)
2. Card serial number
3. Part description
4. Circuit designation, if applicable
5. Keithley part number

5.4 FACTORY SERVICE

If the matrix card is to be returned to Keithley Instruments for repair, perform the following:

1. Complete the service form located at the back of this manual, and include it with the unit.
2. Carefully pack the card in the original packing carton or the equivalent.
3. Write ATTENTION REPAIR DEPARTMENT on the shipping label. Note that it is not necessary to return the matrix mainframe with the card.

5.5 COMPONENT LAYOUT AND SCHEMATIC DIAGRAM

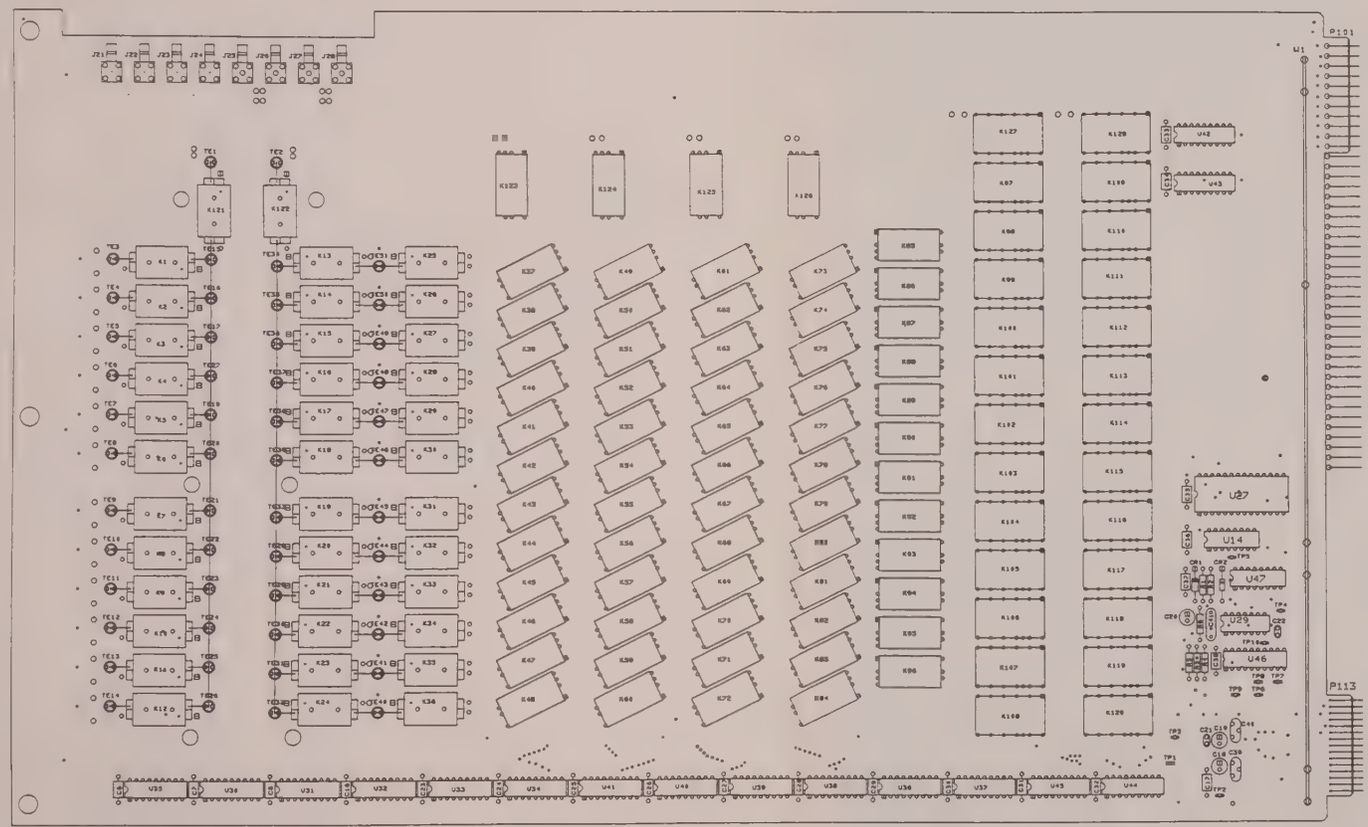
Figure 5-1 is the component layout for the Model 7072. Figure 5-2 shows a schematic diagram of the card on four separate sheets.

TABLE 5-1. MODEL 7072 ELECTRICAL PARTS LIST

CIRCUIT DESIG.	DESCRIPTION	KEITHLEY PART NO.
C18..C20	CAP,10uF,-20+100%,25V,ALUM ELEC	C-314-10
C21,C22	CAP,.01uF,20%,50V,CERAMIC	C-237-.01
C23..C38		
C39,C40	CAP,270pF,20%,100V,CERAMIC/FERRITE	C-386-270P
C41	CAP,.01uF,10%,1000V,CERAMIC	C-64-.01
C6..C8,C16,C17,	CAP,.1uF,20%,50V,CERAMIC	C-365-.1
CR1	DIODE,SILICON,1N4148 (DO-35)	RF-28
CR2	DIODE,SCHOTTKY,1N5711	RF-69
J1...J20	CONN,TRIAX	CS-630
J21-J28	CONN,SMB,MALE	CS-580
K1..K36,K121,	RELAY,REED	RL-106
K122		
K127,K128		
K37..K96,	RELAY,REED,(DPST)	RL-105
K97..K120,	RELAY,(4PST)	RL-104
R1	RES,47K,5%,1/4W,COMPOSITION OR FILM	R-76-47K
R2	RES,10K,5%,1/4W,COMPOSITION OR FILM	R-76-10K
R3	RES,120K,5%,1/4W,COMPOSITION OR FILM	R-76-120K
R4	RES,680,5%,1/4W,COMPOSITION OR FILM	R-76-680
R5	RES,11K,5%,1/4W,COMPOSITION OR FILM	R-76-11K
R6	RES,200,5%,1/4W,COMPOSITION OR FILM	R-76-200
TE1..TE17,	TERMINAL (TEFLON)	TE-97-1
TE19..TE51		
TP1..TP10	CONN,TEST POINT	CS-553
U14	IC,12 STAGE BINARY COUNTER,74HCT4040	IC-545
U27	IC, 64K EPROM, 2764, PROGRAMMED	7072-800
U29	IC,QUAD 2 INPUT NAND,74HCT00	IC-399
U30..U45	IC,8-BIT SERIAL-IN/LTCH DRIVE,UCN-5841A	IC-536
U46	IC,OCTAL BUFFER/LINE DRIVER,74HCT244	IC-483
U47	IC,8 BIT PARALLEL TO SERIAL,74HCT165	IC-548
W1	STIFFENER,BOARD	J-16

TABLE 5-2 MODEL 7072, MECHANICAL PARTS LIST

DESCRIPTION	KEITHLEY PART NO.
CABLE CLAMP	CC-38-4
STANDOFFS	ST-137-1
ASSEMBLY,REAR PANEL	7072-302
CABLE ASSEMBLY	CA-54-1
CAP,PROTECTIVE	CAP-30-1
FASTENER	FA-154-1
HANDLE	HH-33-1
SHIELD,REAR	7071-311
SHIELD,ROW A	7072-305
SHIELD,ROW B	7072-306
STANDOFF	7071-310
SOCKET FOR U27	SO-69



LTR	ECO NO.	REVISION	ENG	DATE
B	12349	RELEASED		9-14-87
C	12566	REVISED		

NOTE:
FOR COMPONENT INFORMATION
REFER TO BILL OF MATERIAL
(7072-000-00).

7072		
MODEL	NEXT ASSEMBLY	QTY.
USED ON		

DO NOT SCALE THIS DRAWING	DIMENSIONAL TOLERANCES UNLESS OTHERWISE SPECIFIED	DATE 1-26-88	SCALE 1:1
KEITHLEY INSTRUMENTS INC. CLEVELAND, OHIO 44139	XX=±.015 ANG.=±1°	DRN. CB	ENG APPR.
	XXX=±.005 FRAC.=±1/64	MATERIAL	
	SURFACE MAX. 63	FINISH	

TITLE: COMPONENT LAYOUT, SEMICONDUCTOR CARD

NO. 7072-100

Figure 5-1. Model 7072 Component Location Drawing, Dwg. No. 7072-100

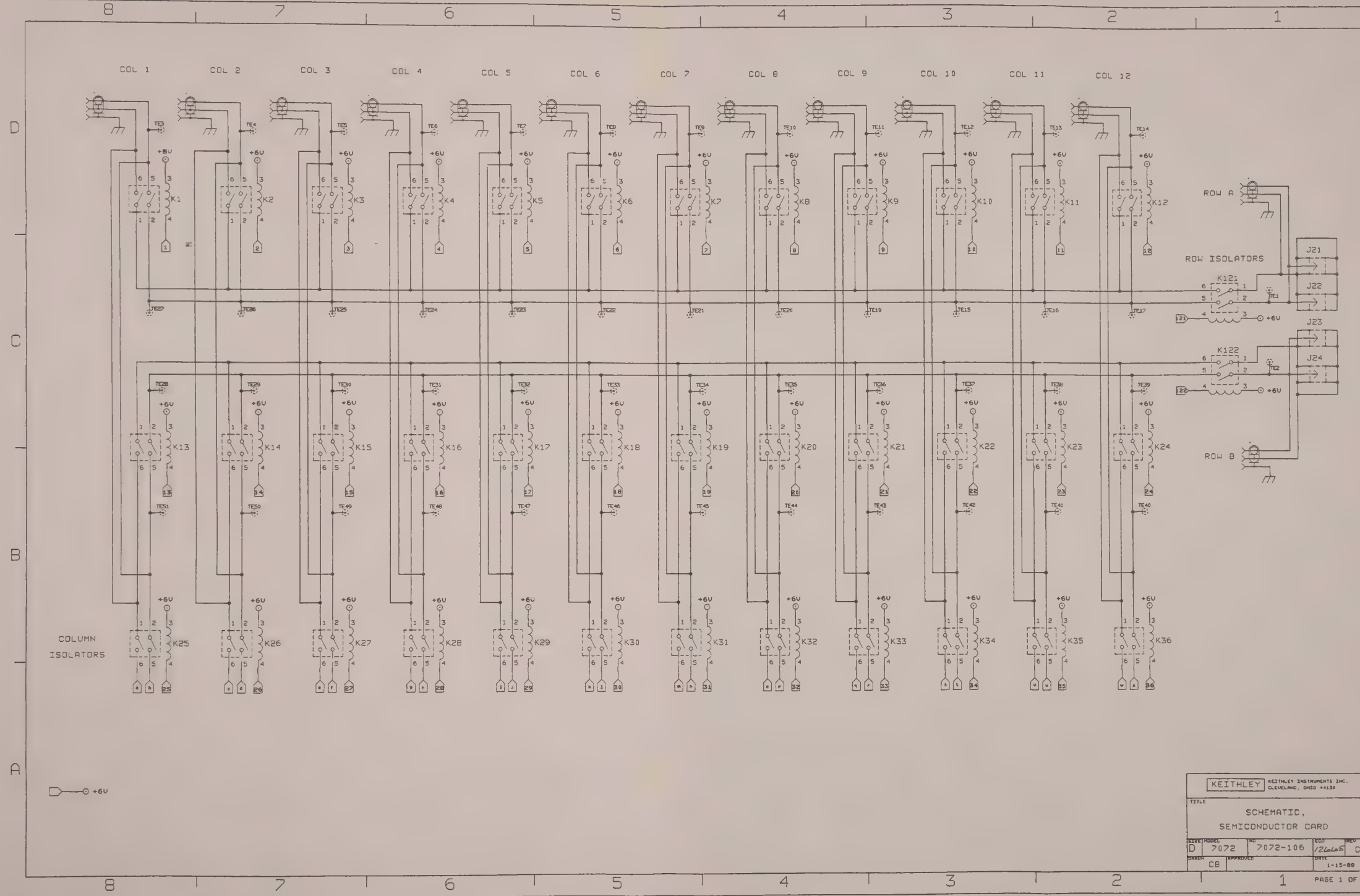


Figure 5-2. Model 7072 Schematic Diagram, Dwg. No. 7072-106 (sheet 1 of 4)

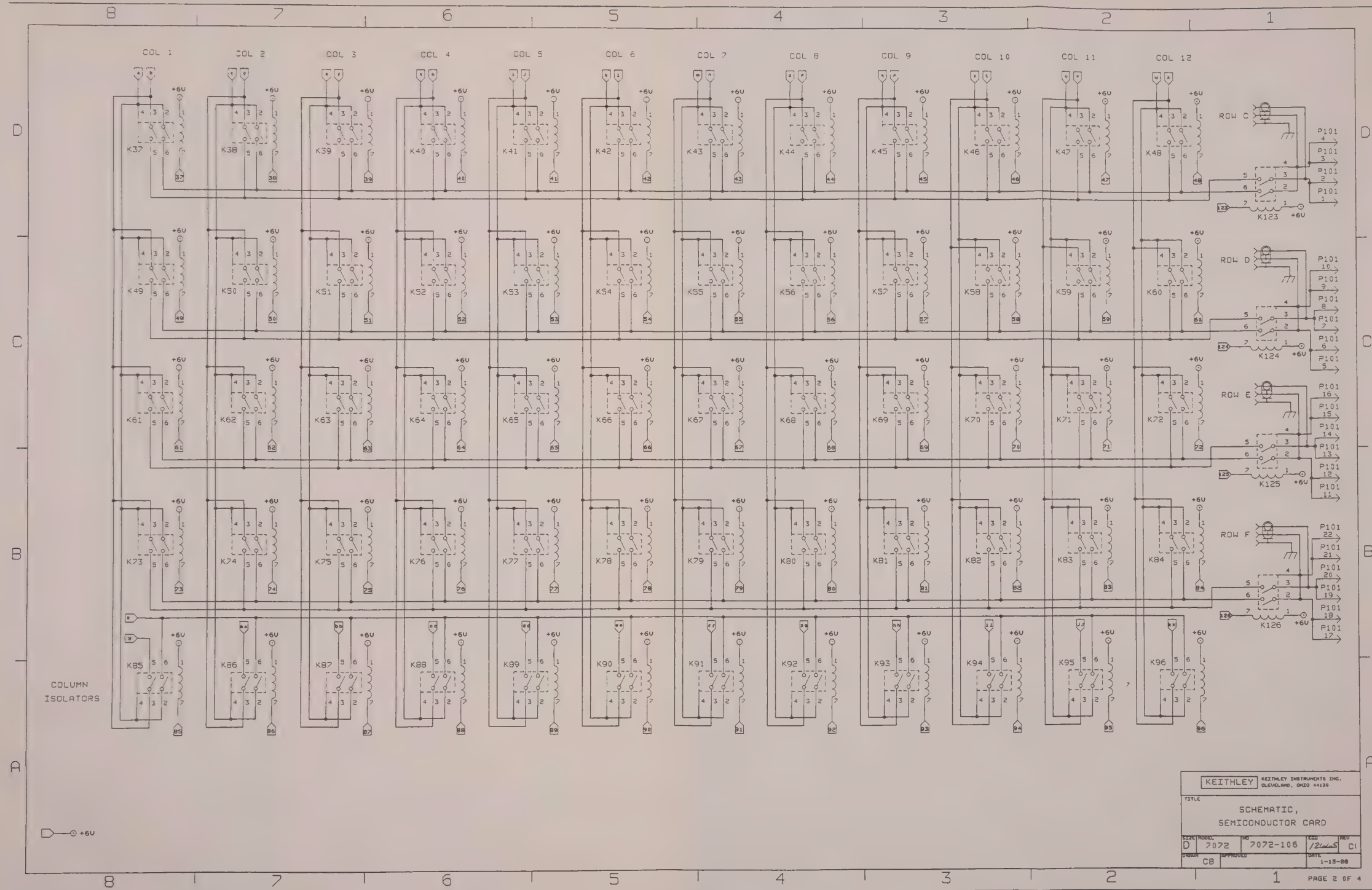


Figure 5-2. Model 7072 Schematic Diagram, Dwg. No. 7072-106 (sheet 2 of 4)

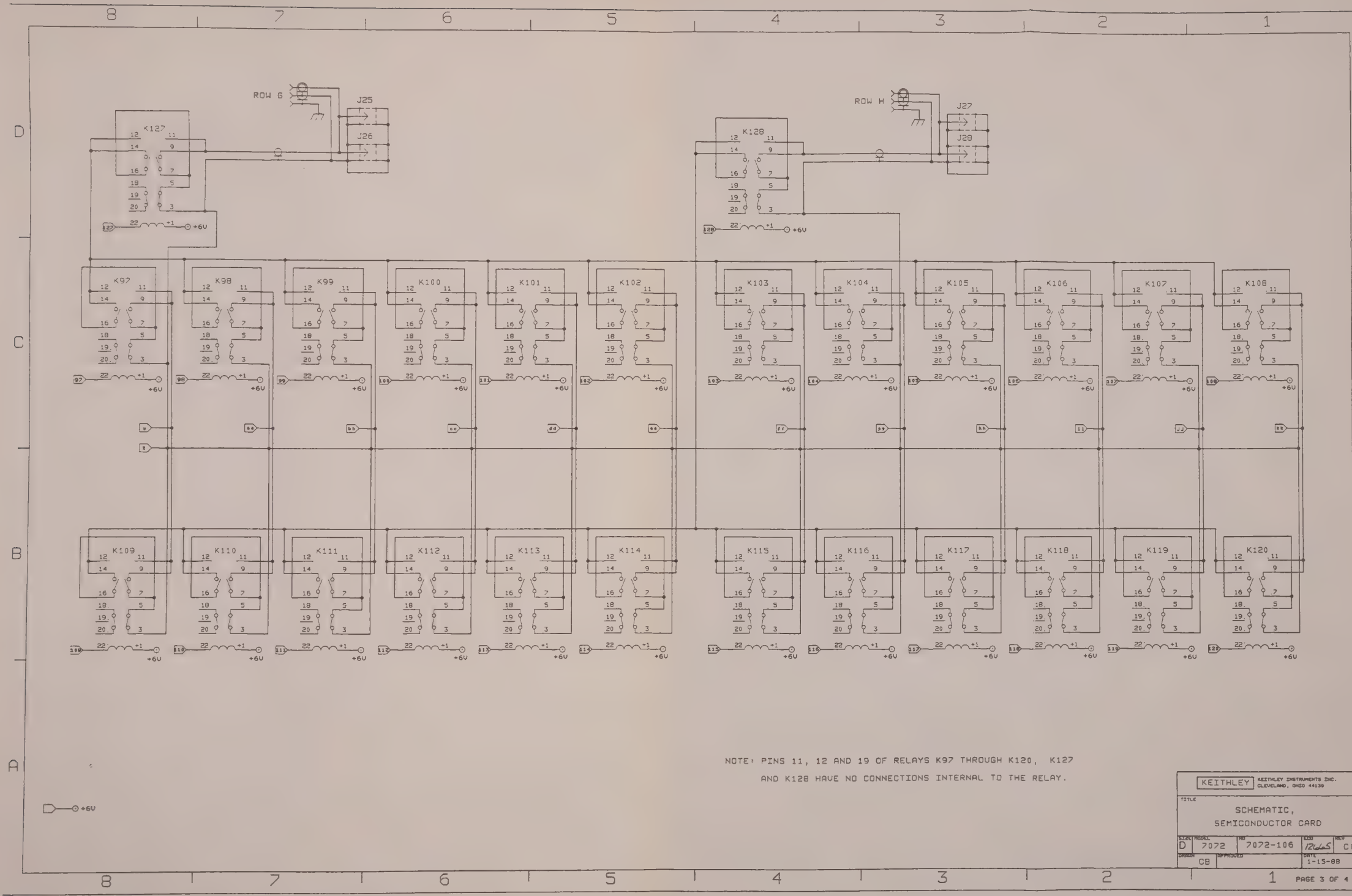


Figure 5-2. Model 7072 Schematic Diagram, Dwg. No. 7072-106 (sheet 3 of 4)

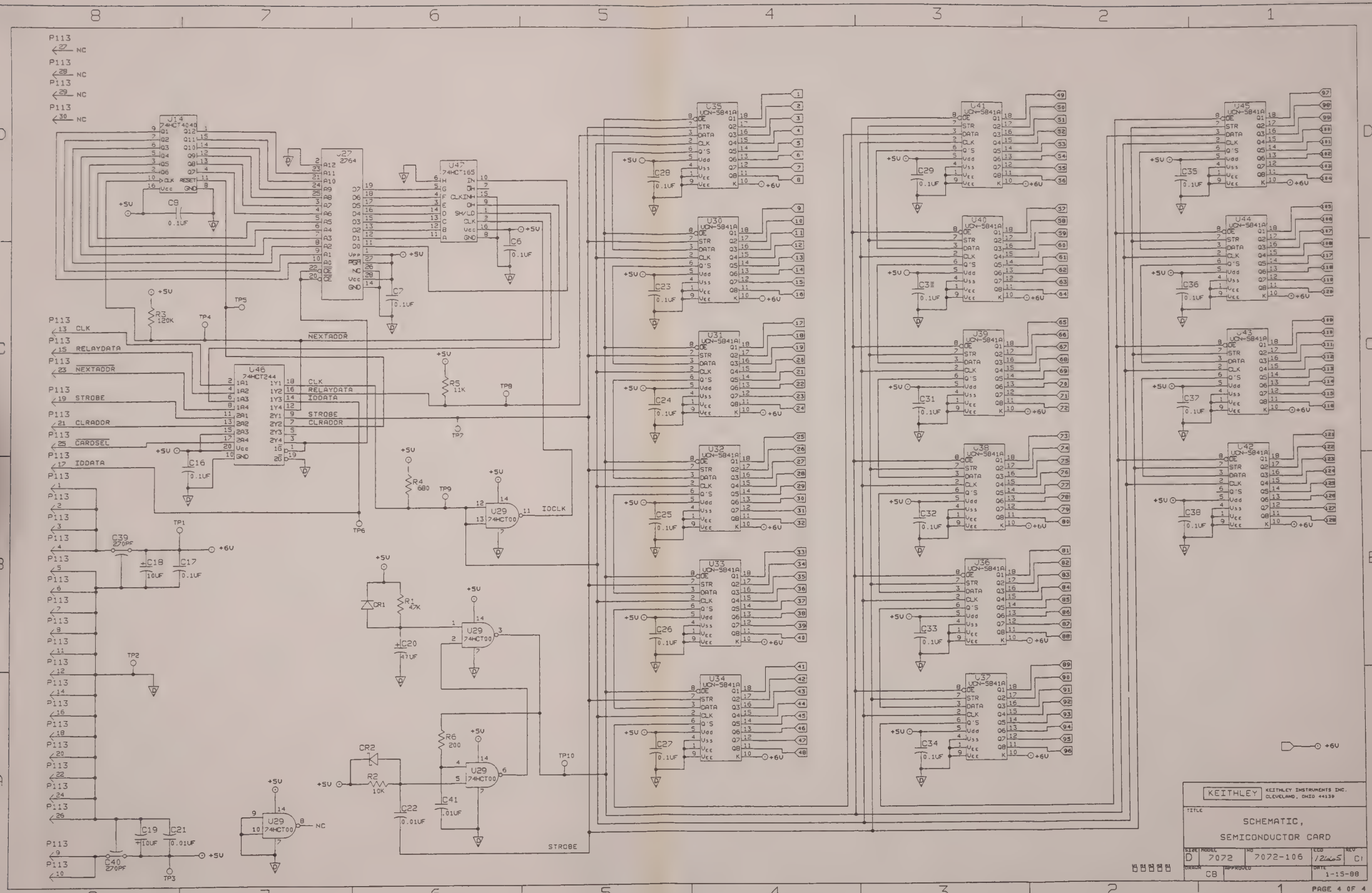


Figure 5-2. Model 7072 Schematic Diagram, Dwg. No. 7072-106 (sheet 4 of 4)

KEITHLEY

Service Form

Model No. _____ **Serial No.** _____ **Date** _____

Name and Telephone No. _____

Company _____

List all control settings, describe problem and check boxes that apply to problem. _____

_____

_____

- ❑ Intermittent
- ❑ IEEE failure
- ❑ Front panel operational
- ❑ Analog output follows display
- ❑ Obvious problem on power-up
- ❑ All ranges or functions are bad
- ❑ Particular range or function bad; specify _____
- ❑ Batteries and fuses are OK
- ❑ Checked all cables

Display or output (check one)

- ❑ Drifts
- ❑ Unstable
- ❑ Overload
- ❑ Unable to zero
- ❑ Will not read applied input

- ❑ Calibration only
- ❑ Data required
- ❑ Certificate of calibration required

(attach any additional sheets as necessary)

Show a block diagram of your measurement system including all instruments connected (whether power is turned on or not). Also, describe signal source.

Where is the measurement being performed? (factory, controlled laboratory, out-of-doors, etc.)

_____

_____

What power line voltage is used? _____ Ambient temperature? _____ °F

Relative humidity? _____ Other? _____

Any additional information. (If special modifications have been made by the user, please describe.)

_____

_____

Be sure to include your name and phone number on this service form.

KEITHLEY

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